

Compal Confidential

STORM3 M/B Schematic

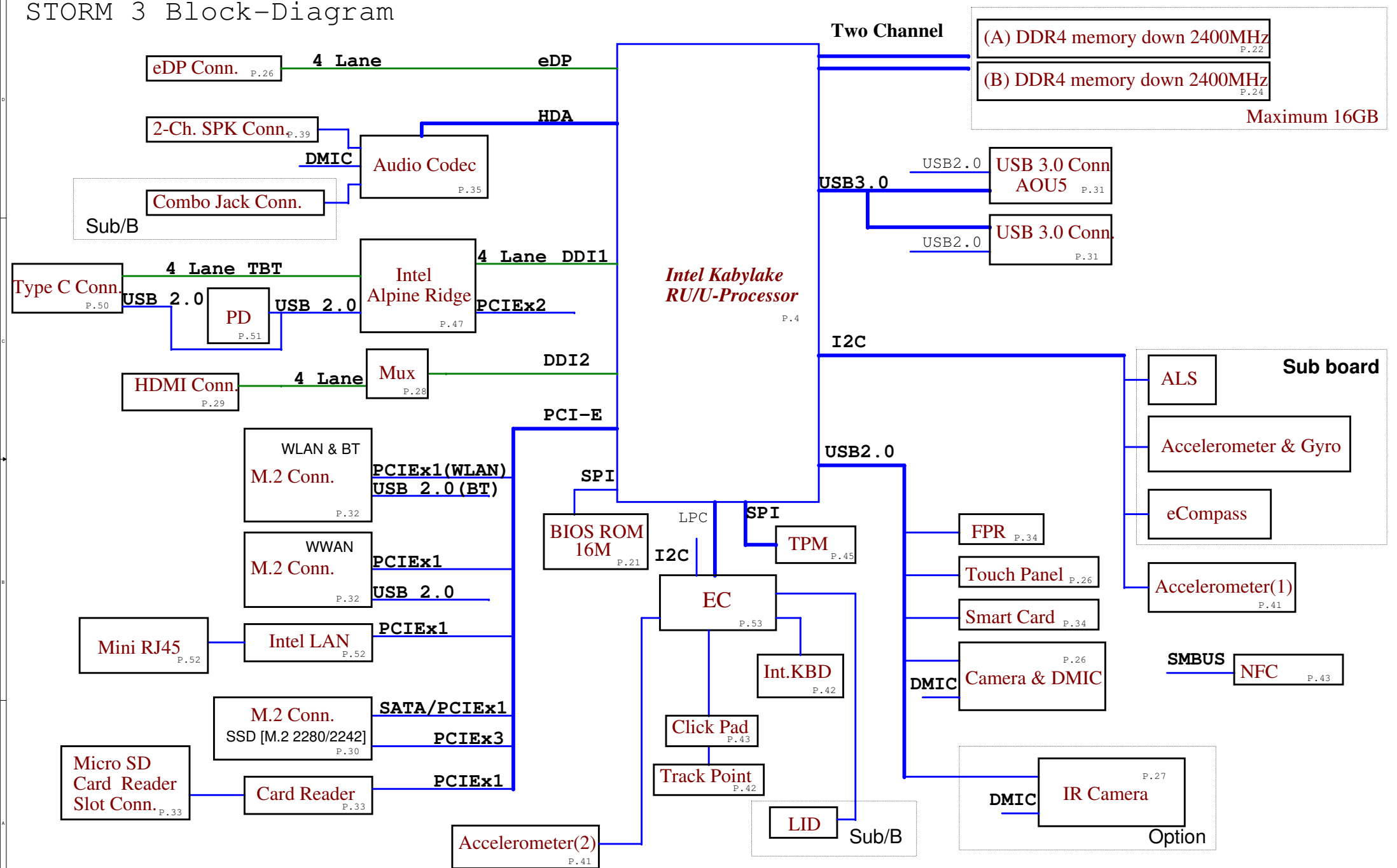
LA-F421P

Rev: 1.0_ B

2017.10.23

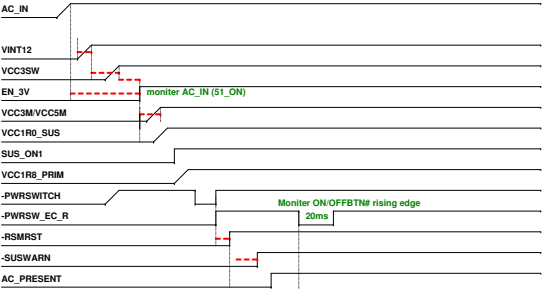
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STORM 3 Block-Diagram

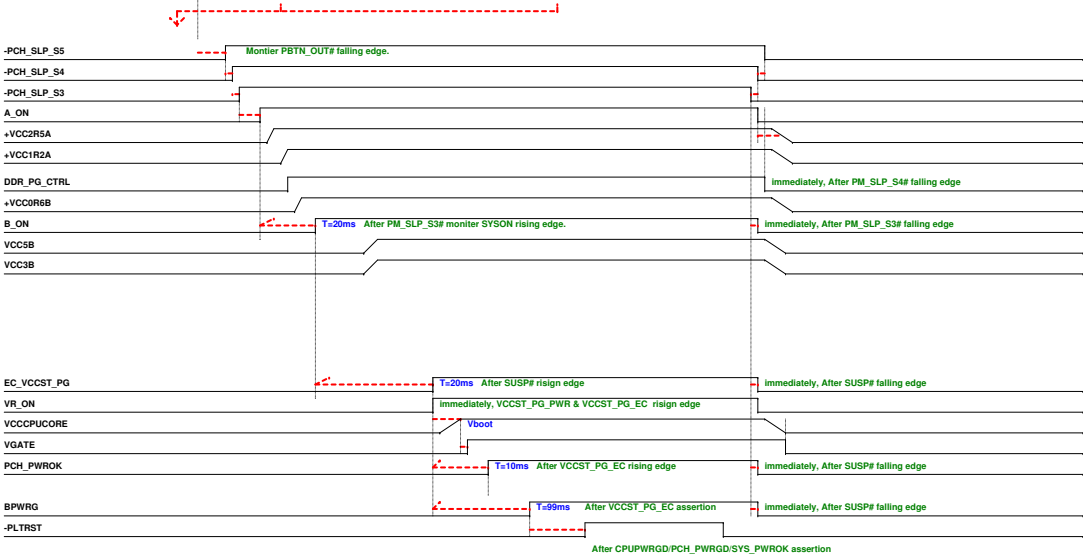
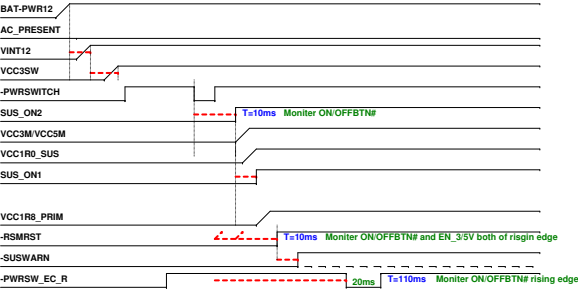


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[AC Mode]

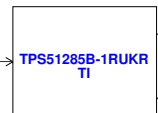
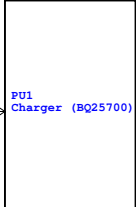


[DC Mode]



Storm3 Power tree

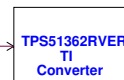
VINT20



VCC5M / 7A
VCC3M / 7A



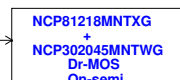
VCC2R5A / 0.8A
VCC1R8_SUS / 0.8A



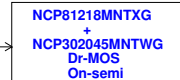
VCC1R0_SUS_P / 7.12A



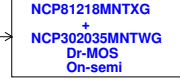
VCC1R2A / 6.4A
VCC0R6B / 0.8A



VCCCPUCORE
U22: 21A
U42: 42A

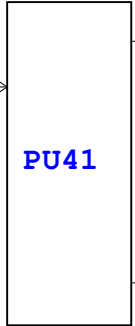


VCCGFXCORE_I / 18A



VCCSA / 4A

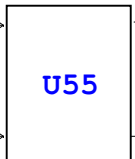
VINT12



VCC5M

VCC3M

- U143 VCCST
- P0151 VCC2R5A
- P0118 VCC1R2A
- P0145 VCC1R8 PRIM
- U53 USB_PWR_S2
- U88 USB_PWR_S1
- R9570 VCC5M_BUTTON
- J9237 VCC5M_PD
- P0154 VCC3_SUS
- F31 VCC3M_PEN
- F34 VCC3M_SENS_CN
- F39 VCC3M_IR
- F25 VCC3M_KEY_CONN
- R9309 VCC3M_BUTTON
- R2485 VCC3M_PCH
- R9406 VCC3_TBT
- R9369 VCC3M_PD
- U19 VCC3WLAN
- U153 VCC3LAN

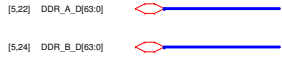


VCC5B

VCC3B

- U110 VCC5B_HDMI
- F40 VCC5B_IR
- F35 VCC5B_CN
- F23 VCC5_TP
- F4 VCC5B_F4
- F15 FUSEVCC5B
- R2031 VCC5B_CODEC
- R2015 VCC5BA
- R2463 VCC3B_PS8337B
- J9240 VCC3WAN
- F24 VCC3B_TOUCH_CN
- F17 FUSEVCC3B
- F8 FUSEVCC3FP
- F41 VCC3B_IR
- R2029 VCC3B_CODEC
- U9 VCC3P
- R2472 VCC3B_RT55236S



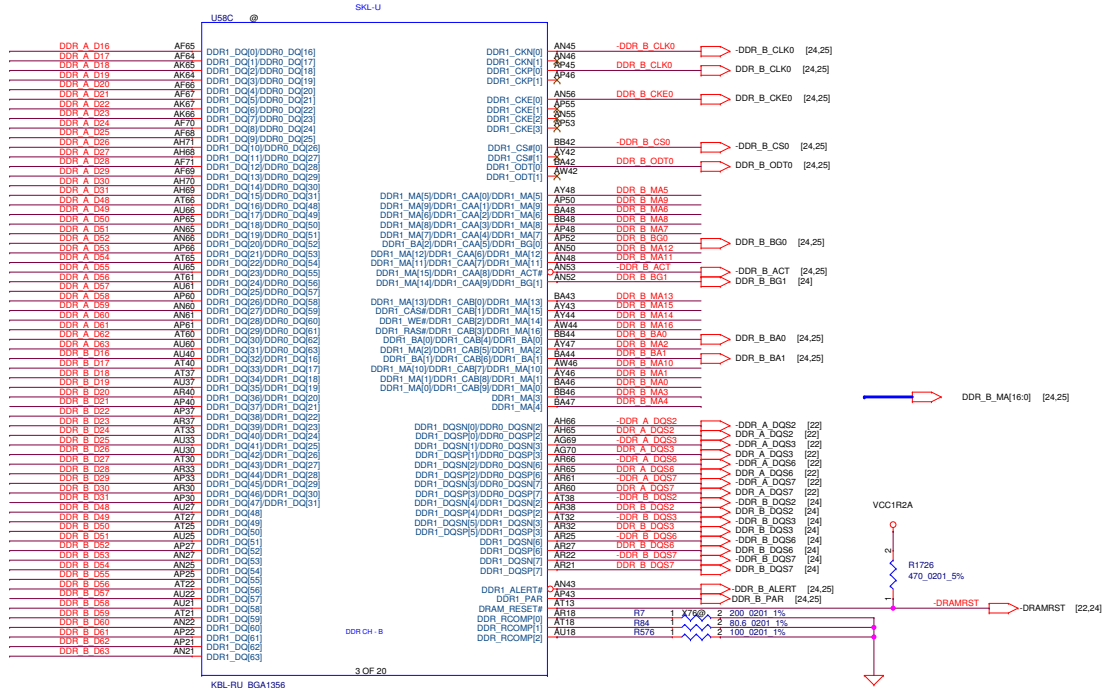


TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AF71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AT22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC

LOGIC



TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG69	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

LOGIC

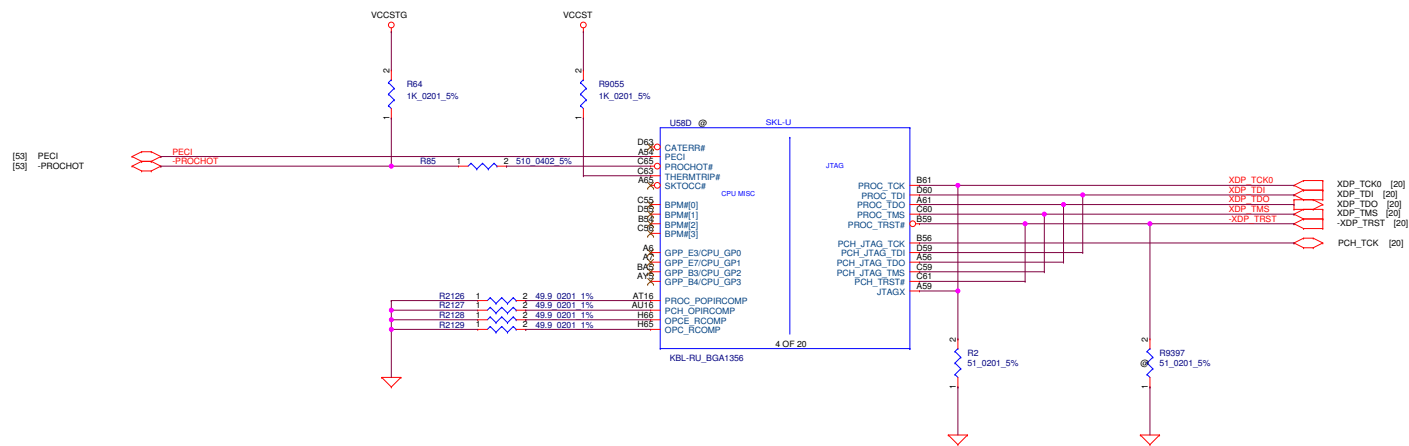
	SDP	DDP
R7	200 1%	121 1%

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

LOGIC



SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

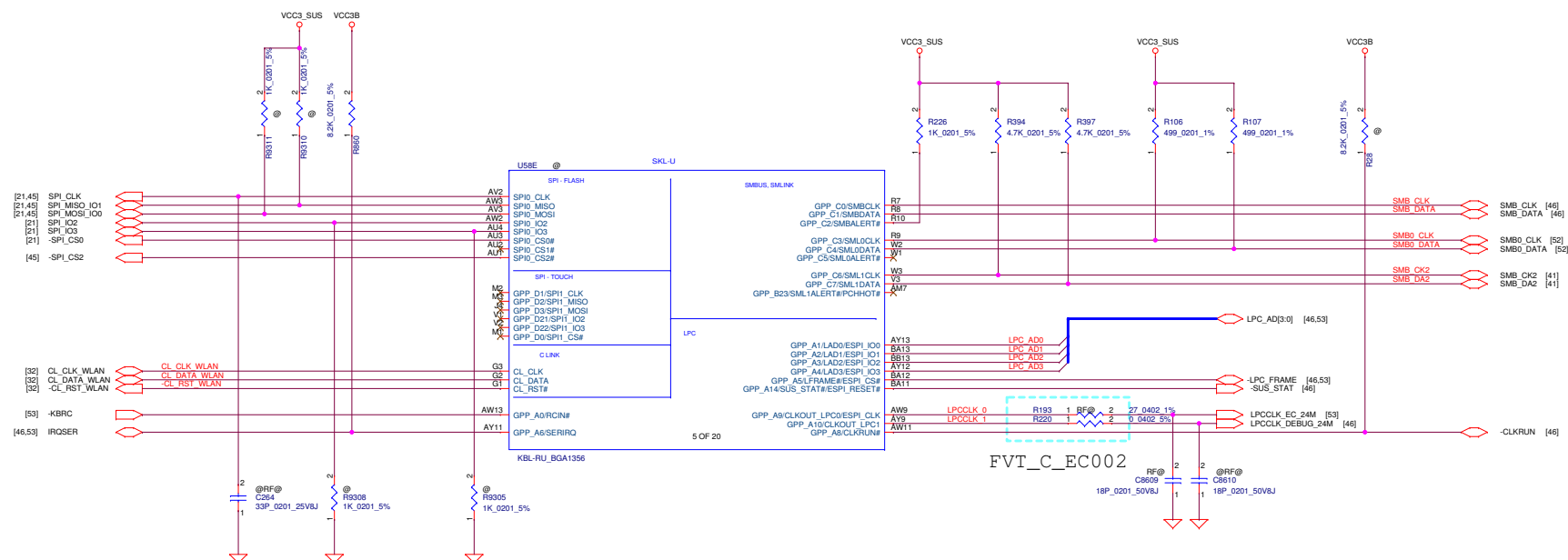
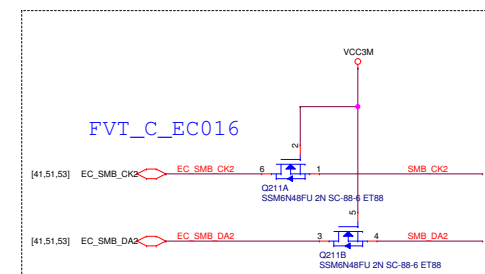
SPI0_MISO (JTAG ODT Diable)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

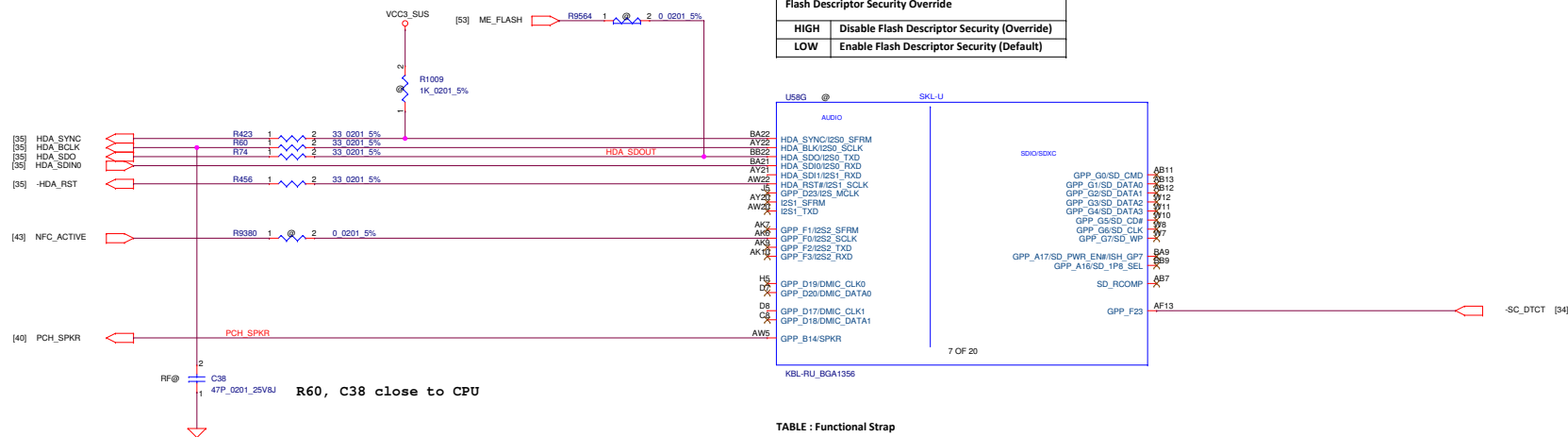
← LOGIC



SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

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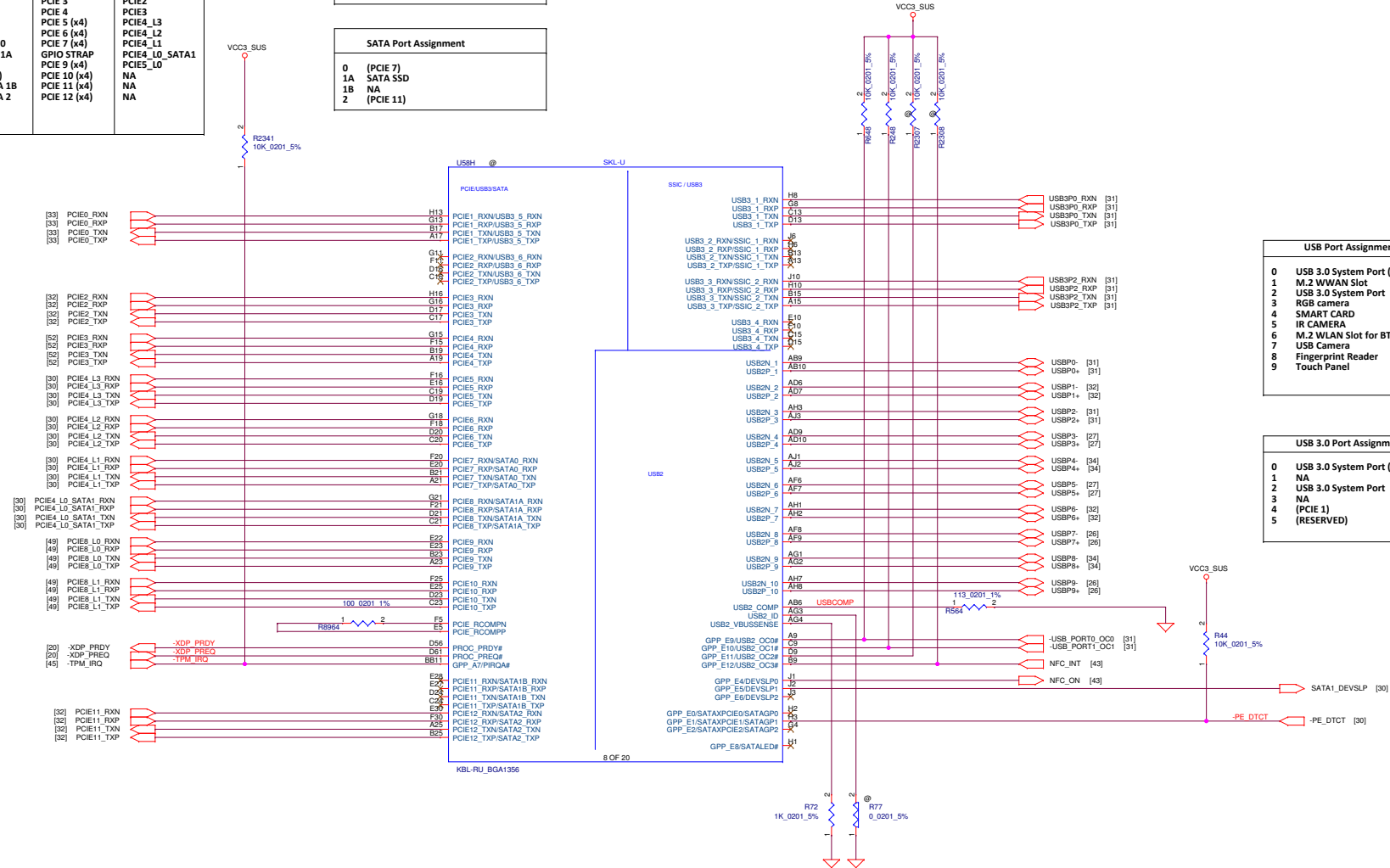
Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	SSIC	SSIC
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1	PCIE0
Port 6	USB3 6/PCIE 2	USB3 6	USB3P5
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE2
Port 8	PCIE 4 (GbE)	PCIE 4	PCIE3
Port 9	PCIE 5 (GbE)	PCIE 5 (x4)	PCIE4_L3
Port 10	PCIE 6	PCIE 6 (x4)	PCIE4_L2
Port 11	PCIE 7/SATA 0	PCIE 7 (x4)	PCIE4_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE4_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x4)	PCIE5_L0
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	NA
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	NA
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	NA

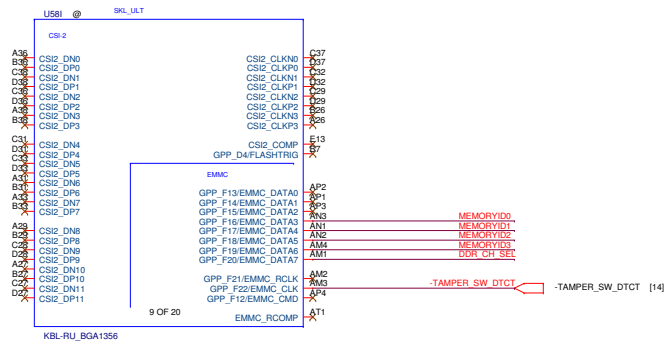
PCIe Port Assignment	
0	MEDIA CARD
2	M.2 WLAN Slot Port 0 for WLAN
3	GbE PHY
4 (x4)	PCIe SSD
8	Thunder bolt
11	WWAN

SATA Port Assignment	
0	(PCIE 7)
1A	SATA SSD
1B	NA
2	(PCIE 11)

USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	M.2 WWAN Slot
2	USB 3.0 System Port
3	RGB camera
4	SMART CARD
5	IR CAMERA
6	M.2 WLAN Slot for BT
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	NA
2	USB 3.0 System Port
3	NA
4	(PCIE 1)
5	(RESERVED)

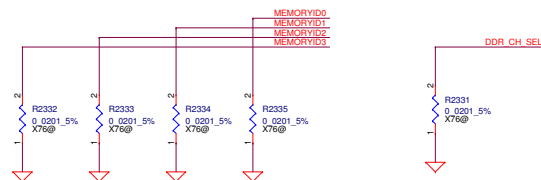




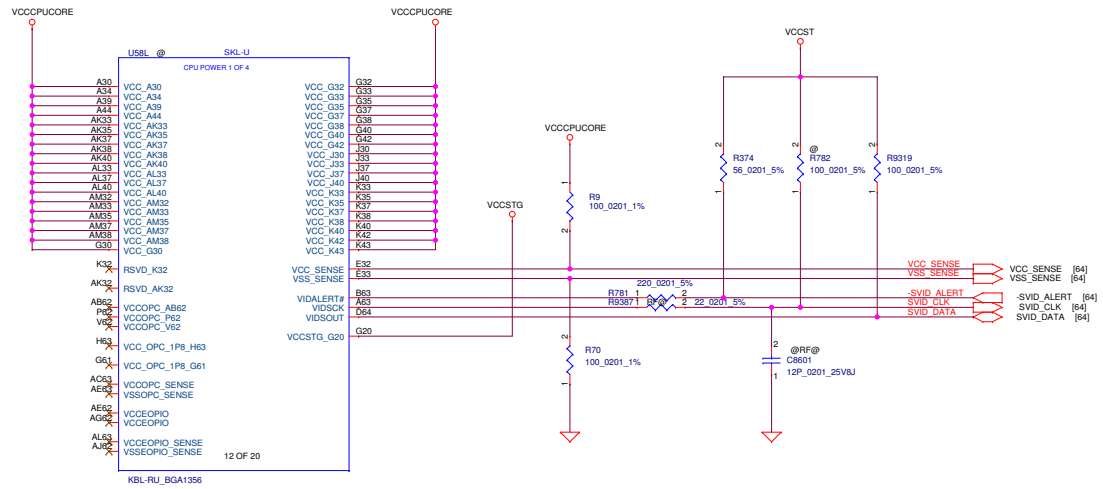
TABLE

MEMORY[3..0]	U125, U126, U127, U128, U129, U130, U131, U132			R7 (Rcomp)
1111B	Samsung K4A8G165WC-BCRC	8Gbit SDP	4GB	200 1%
1110B	Samsung K4AAG165WB-MCRC	16Gbit DDP	8GB	121 1%
1101B	Hynix H5AN8G6NAFR-UHC	8Gbit SDP	4GB	200 1%
1011B	Hynix H5ANAG6NAMR-UHC	16Gbit DDP	8GB	121 1%
0111B	Micron MT40A512M16JY-083E:B	8Gbit SDP	4GB	200 1%
1100B	Micron MT40A1G16WBU-083E:B	16Gbit DDP	8GB	121 1%

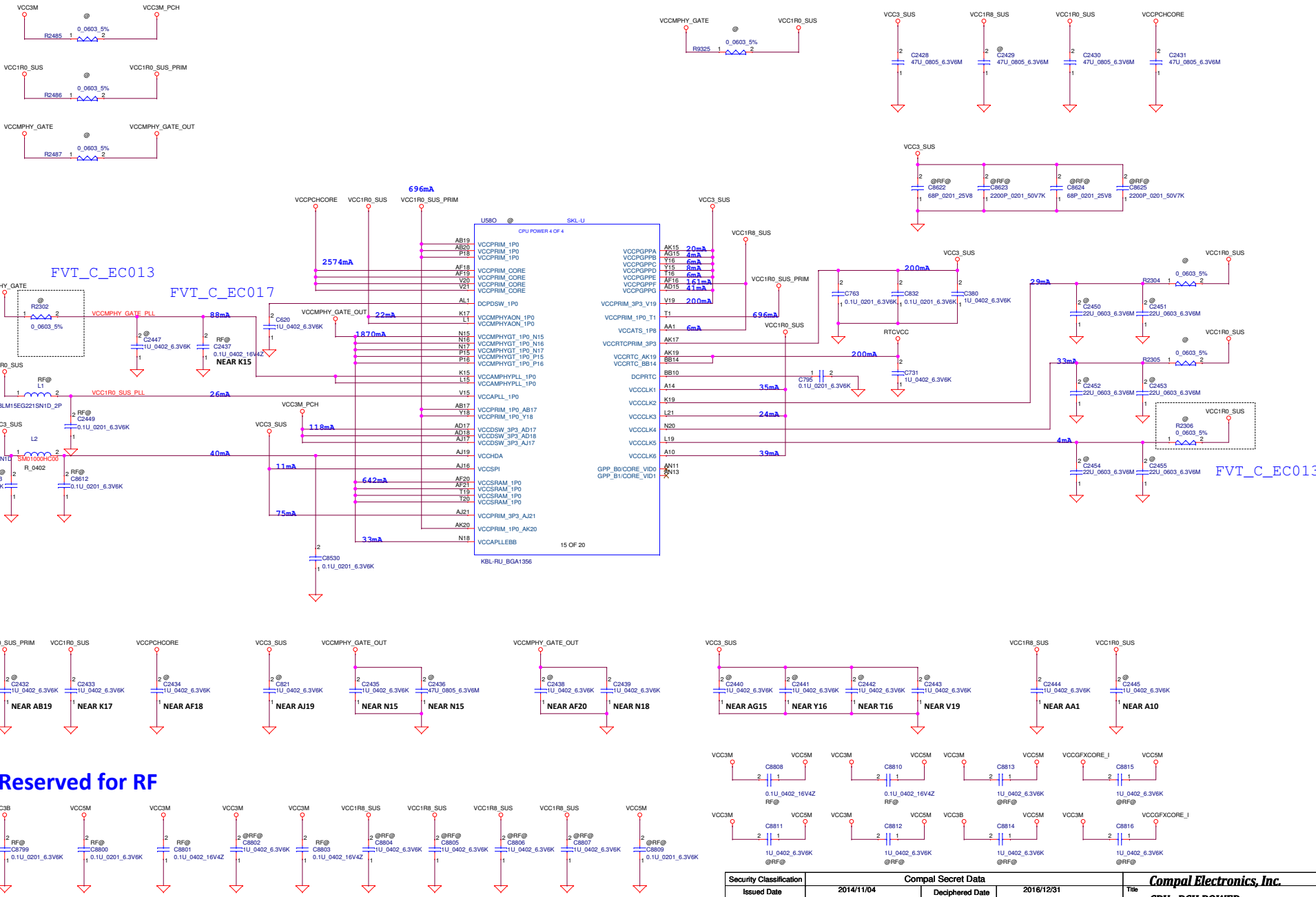
	2CH	1CH
R2331	NC	Mount



VCC I (Max) : 32A (Dual Core)
64A (Qual Core)

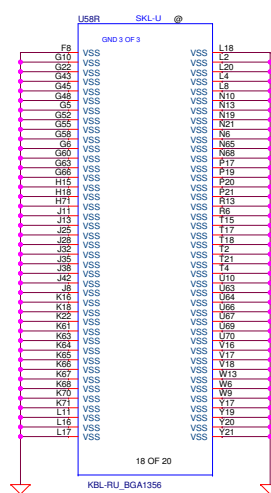
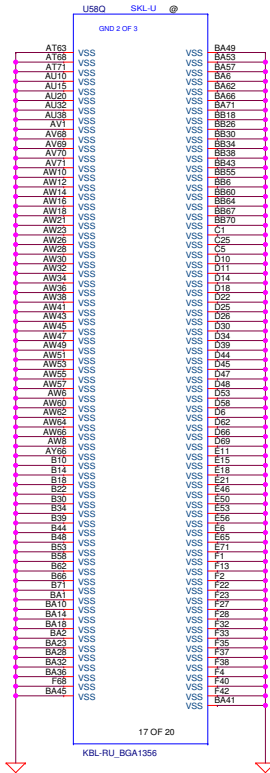
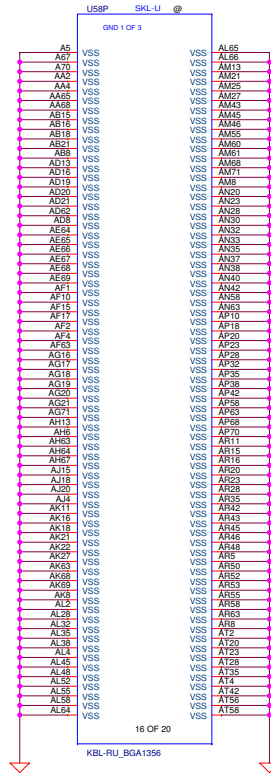


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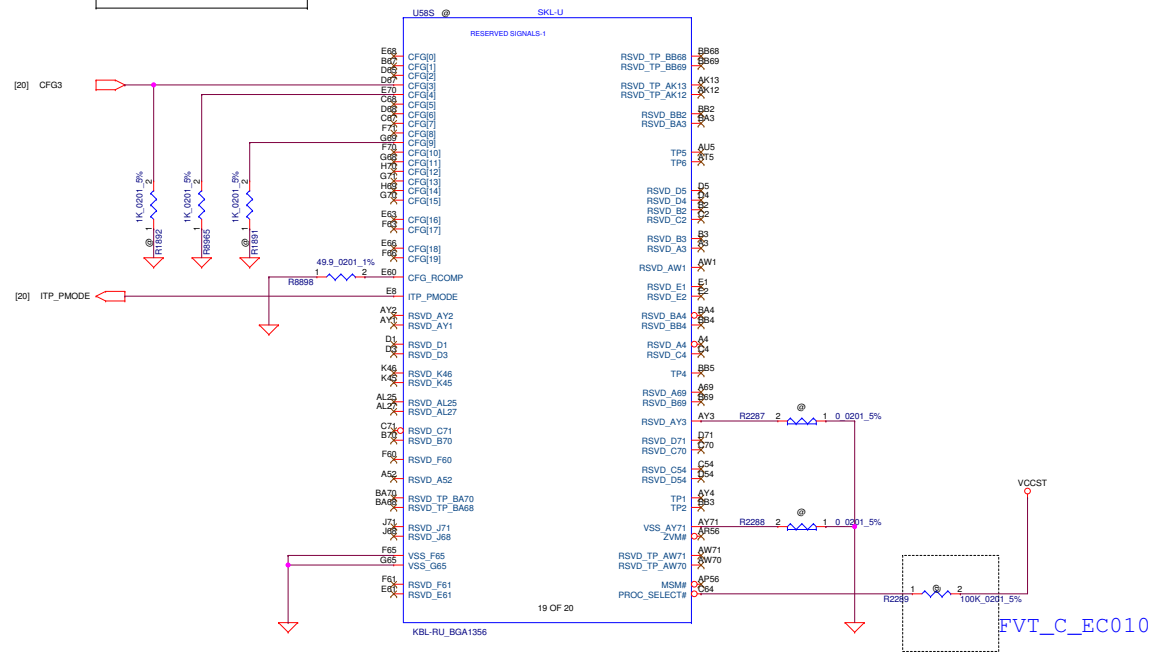
TABLE

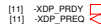
CFG0 : Stall Reset Sequence
after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG3 : MSR Privacy Bit Feature
1 : MSR (C80h) bit[0] setting
0 : MSR (C80h) bit[0] overridden

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled





Logic	Ref Des	Merged	DCI 2.0
Page 7	R2559	ASM	NO_ASM
Page 18	R1982	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	S588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM

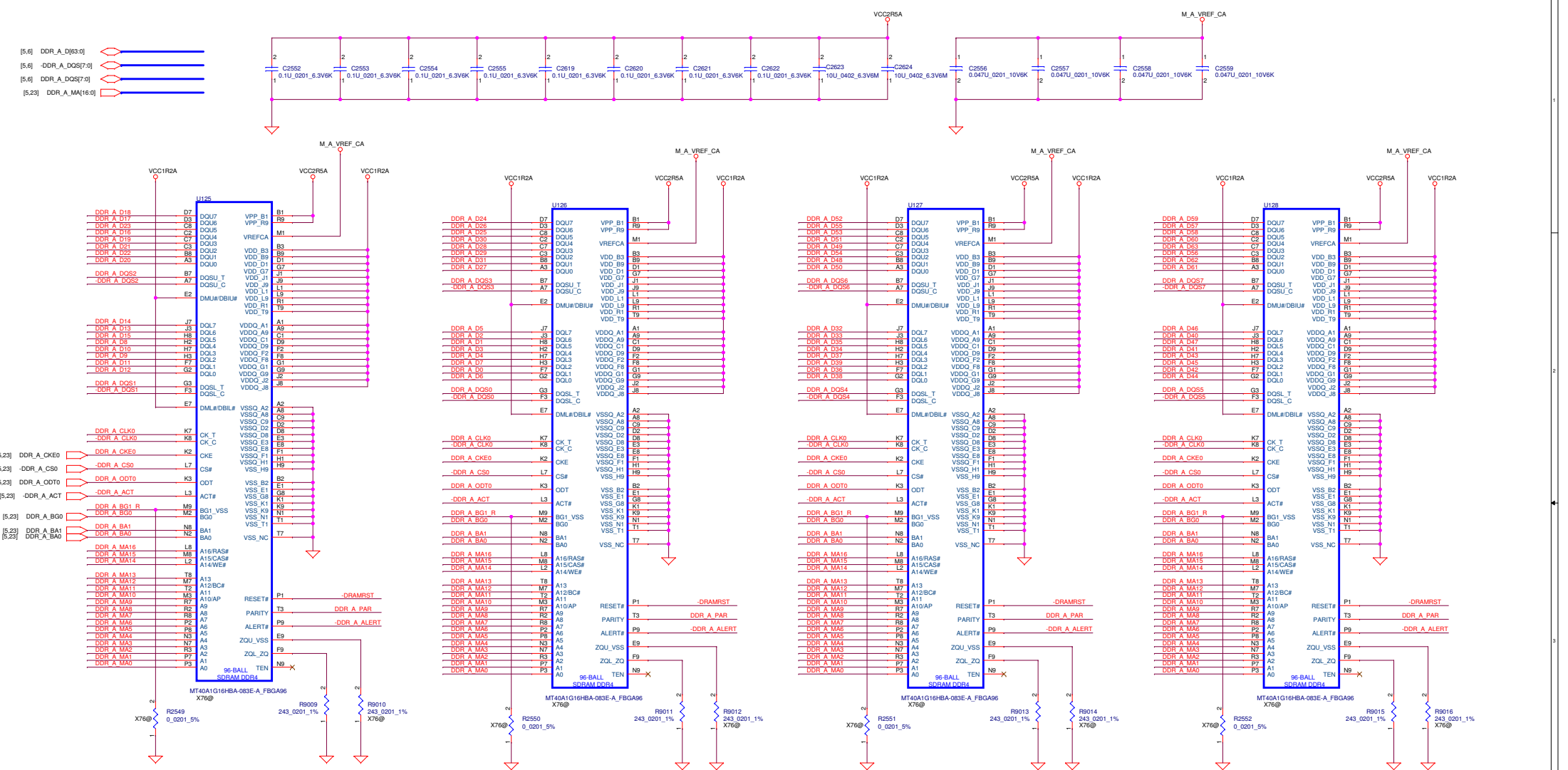
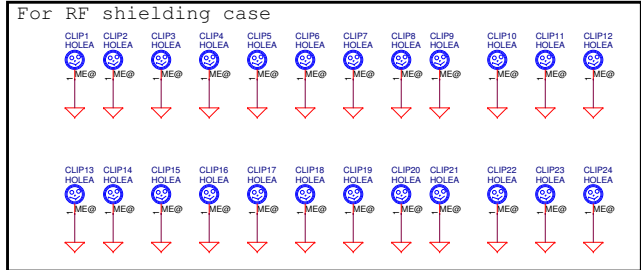
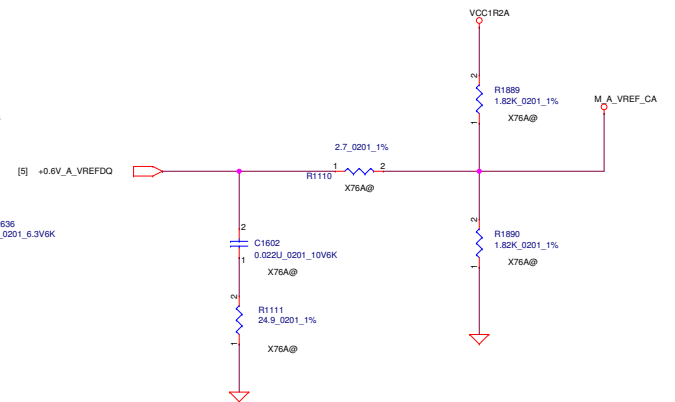
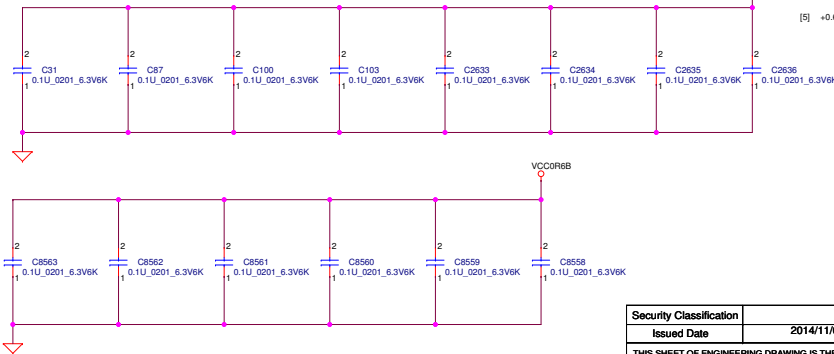
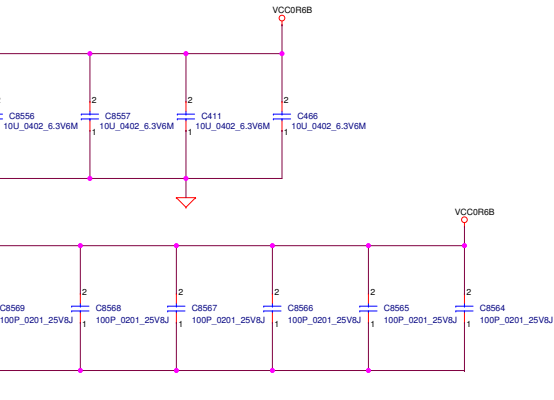
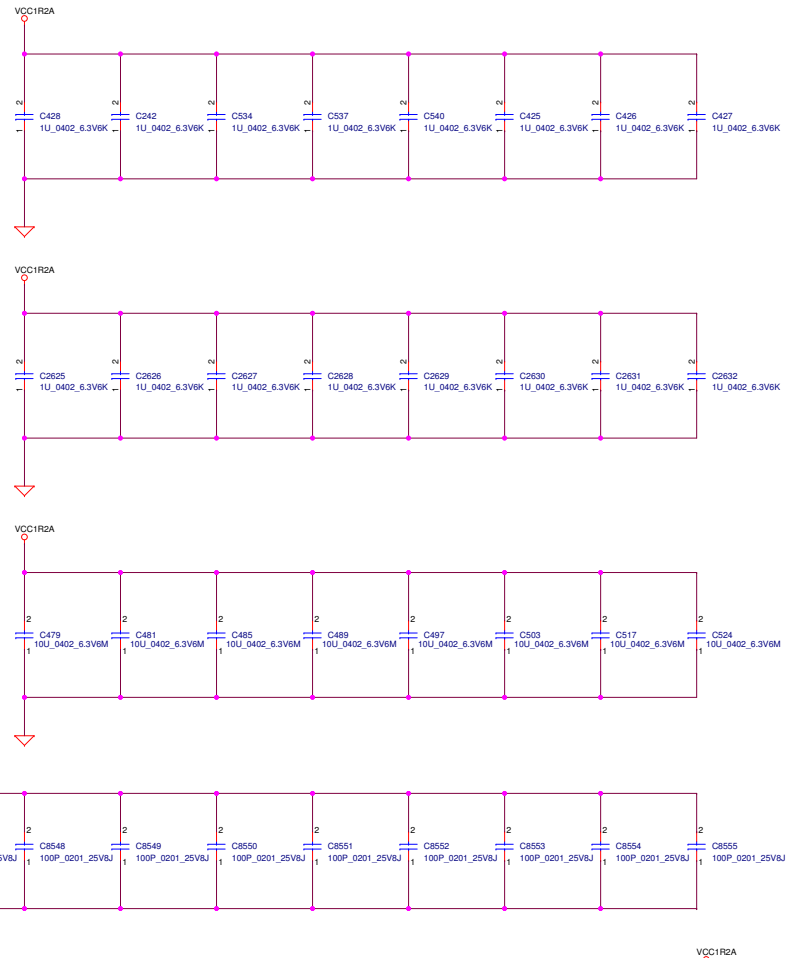
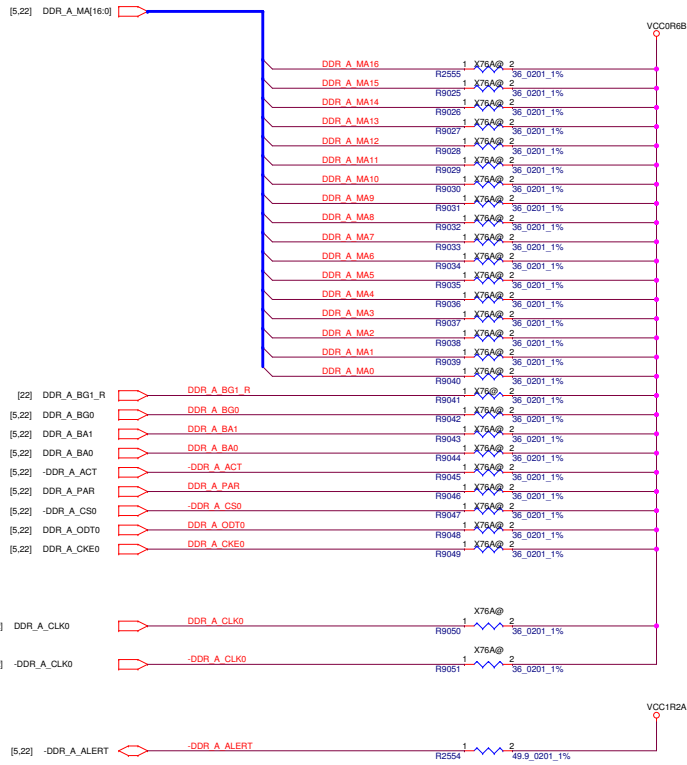


TABLE			
		SDP	DDP
[5.23] DDR_A_CLK0	DDR_A_CLK0	ASM	NA
	R2549	ASM	NA
	R2550	ASM	NA
[5.23] -DDR_A_CLK0	-DDR_A_CLK0	ASM	NA
	R2551	ASM	NA
	R2552	ASM	NA
[5] DDR_A_BG1	DDR_A_BG1	NA	ASM
	R2553	NA	ASM
	R9041	NA	ASM
[5.24] -DRAMRST	-DRAMRST	0_5%	243_1%
	R9010	0_5%	243_1%
	R9012	0_5%	243_1%
	R9014	0_5%	243_1%
[5.23] DDR_A_PAR	DDR_A_PAR	0_5%	243_1%
	R9016	0_5%	243_1%
[5.23] -DDR_A_ALERT	-DDR_A_ALERT	0_5%	243_1%
	R9016	0_5%	243_1%

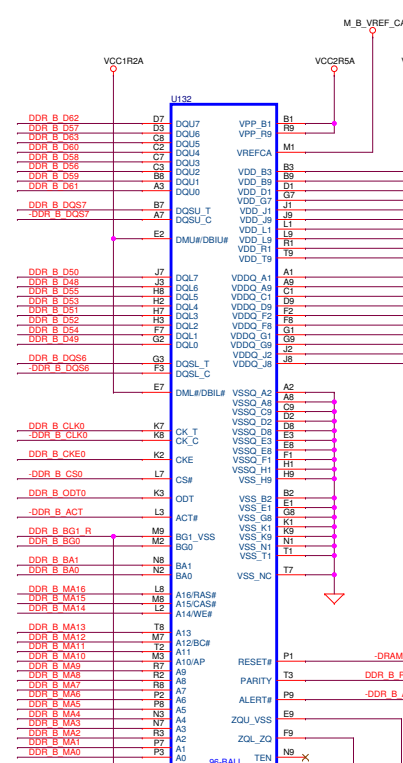
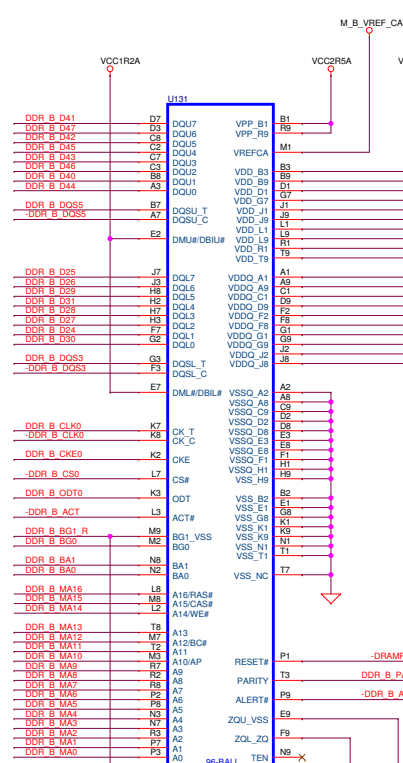
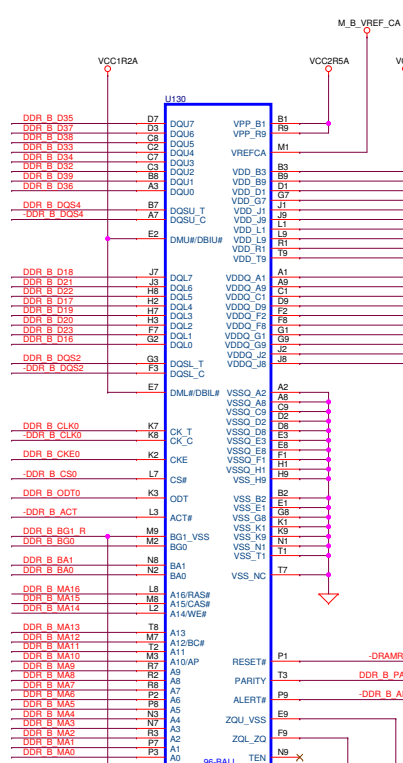
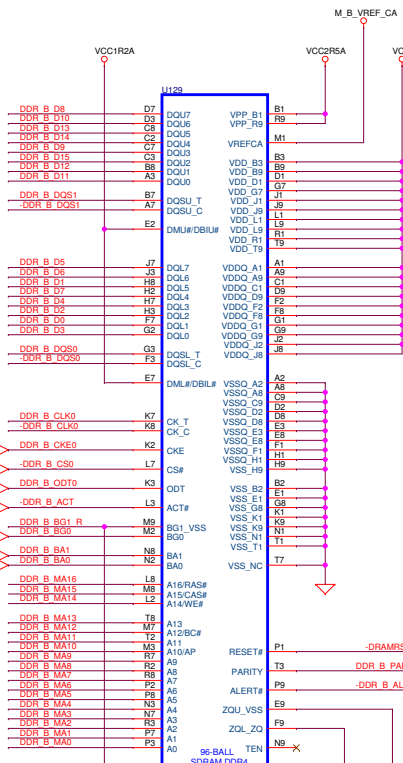
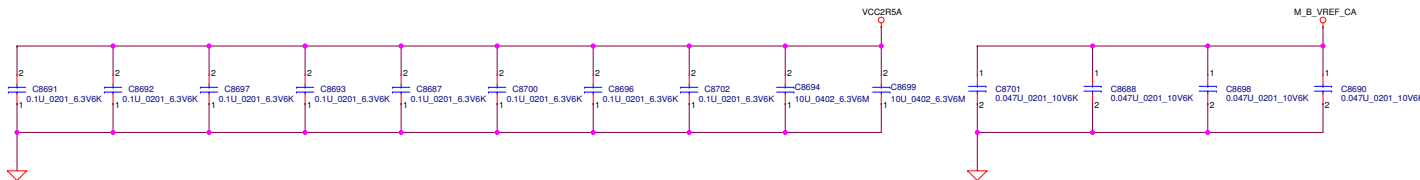


FVT_C_EC006



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		Document Number		Rev	
		Customer		1.0	
		LA-F421P			
		Date		Monday, October 23, 2017	

[5,6] DDR_B_D[63:0]
[5,6] -DDR_B_DQS[7:0]
[6,25] DDR_B_MA[16:0]

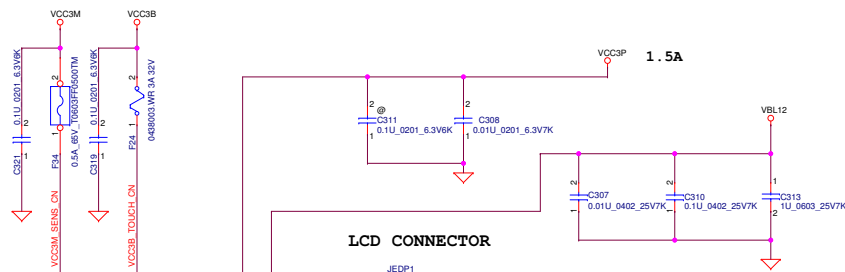
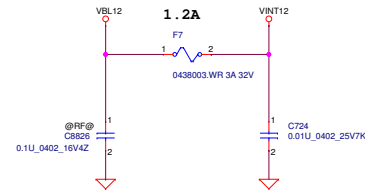
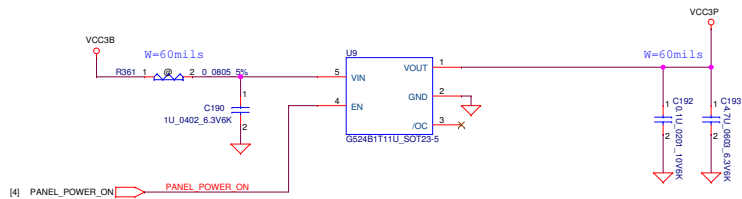


TABLE

	SDP	DDP
R9516	ASM	NA
R9520	ASM	NA
R9523	ASM	NA
R9528	ASM	NA
R9515	NA	ASM
R9556	NA	ASM
R9517	0_5%	243_1%
R9521	0_5%	243_1%
R9524	0_5%	243_1%
R9530	0_5%	243_1%

The schematic diagram illustrates the DDR4 Base Memory CH-B (2/2) circuit. It features several signal traces and power planes. The signal traces include DDR_B_MA16 through DDR_B_MA0, DDR_B_BG1_R through DDR_B_CKE0, DDR_B_CLK0, and -DDR_B_ALERT. The power planes are VCC1R2A and VCC0R6B. Various capacitors are shown with their values and pin numbers. The diagram is labeled with component values and pin numbers.

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LCD CONNECTOR

JEDP1

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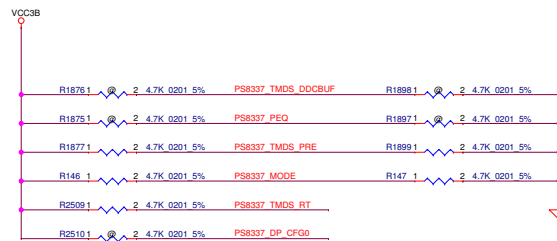
55

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51



SW (DDI_PRIORITY1)	
L	DP Port has higher priority when both ports are plugged
H	TMDS Port has higher priority when both ports are plugged

TMD5 DDCBUF (INT PD)	R1876	R1898	
DDC Active Buffer	ASM	NO_ASM	
DDC Pass Through w/ PU	ASM	ASM	
DDC Pass Through w/o PU	NO_ASM	NO_ASM	← LOGIC

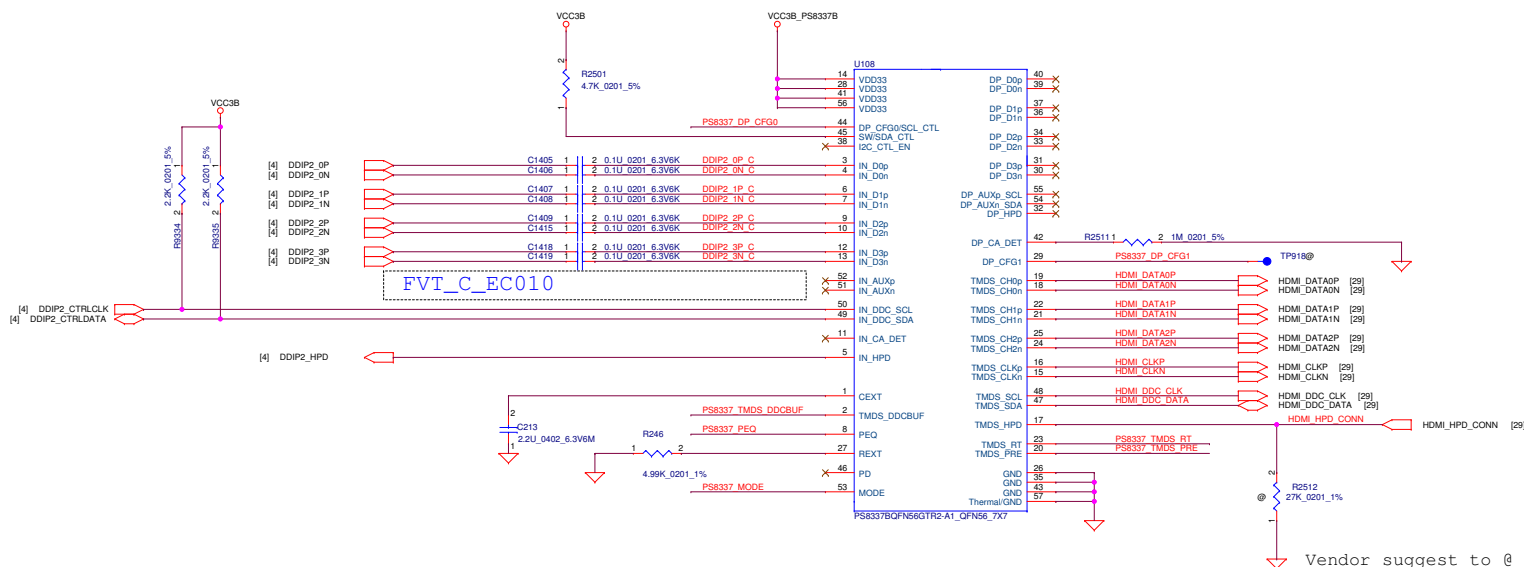
PEQ (INT PD)	R1875	R1897	
HEQ 15dB	ASM	NO_ASM	
LLEQ 5dB	ASM	ASM	
LEQ 12dB	NO_ASM	NO_ASM	← LOGIC

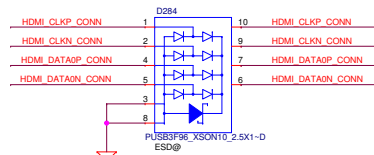
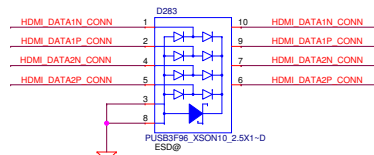
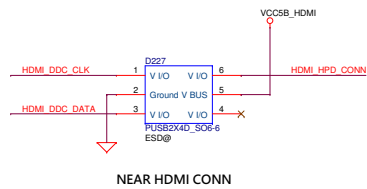
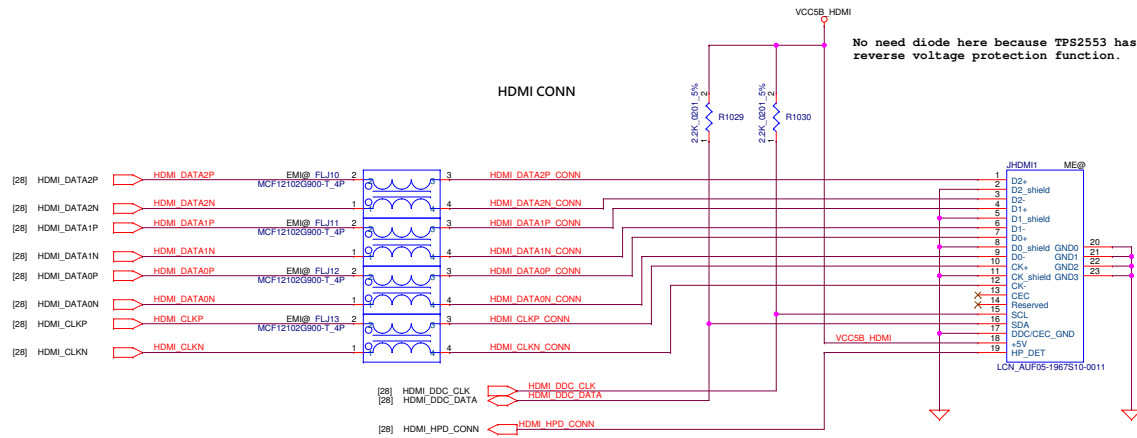
TMD5 PRE (INT PD)	R1877	R1899	
1.5dB	ASM	NO_ASM	
3.0dB	ASM	ASM	← LOGIC
0dB	NO_ASM	NO_ASM	

MODE (INT PD)	R146	R147
Auto HDMI ID disable	ASM	NO_ASM
Auto HDMI ID enable	ASM	ASM
Control HDMI ID disable	NO_ASM	NO_ASM

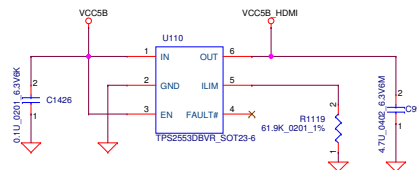
← LOGIC

TMD5 RT (INT PD)	R2509
OD w/ termination	ASM
OD	NO_ASM

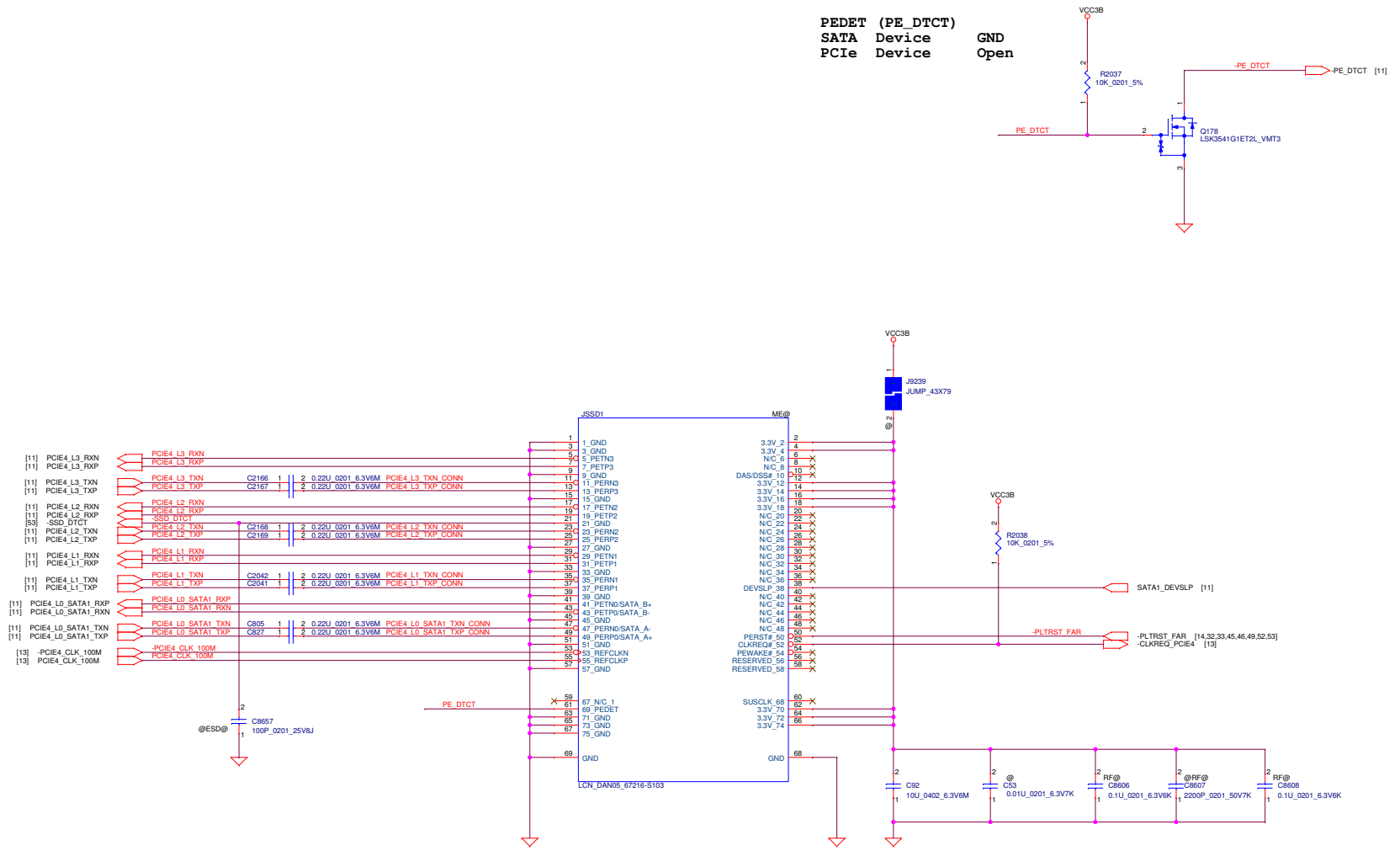




Current Limit Target : 400mA
Requirement : 300mA
HDMI Spec : 50mA - 500mA



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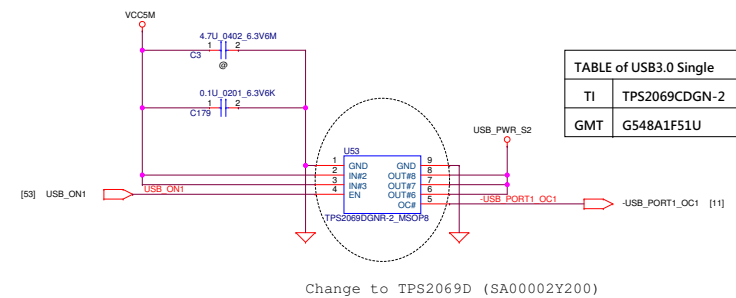
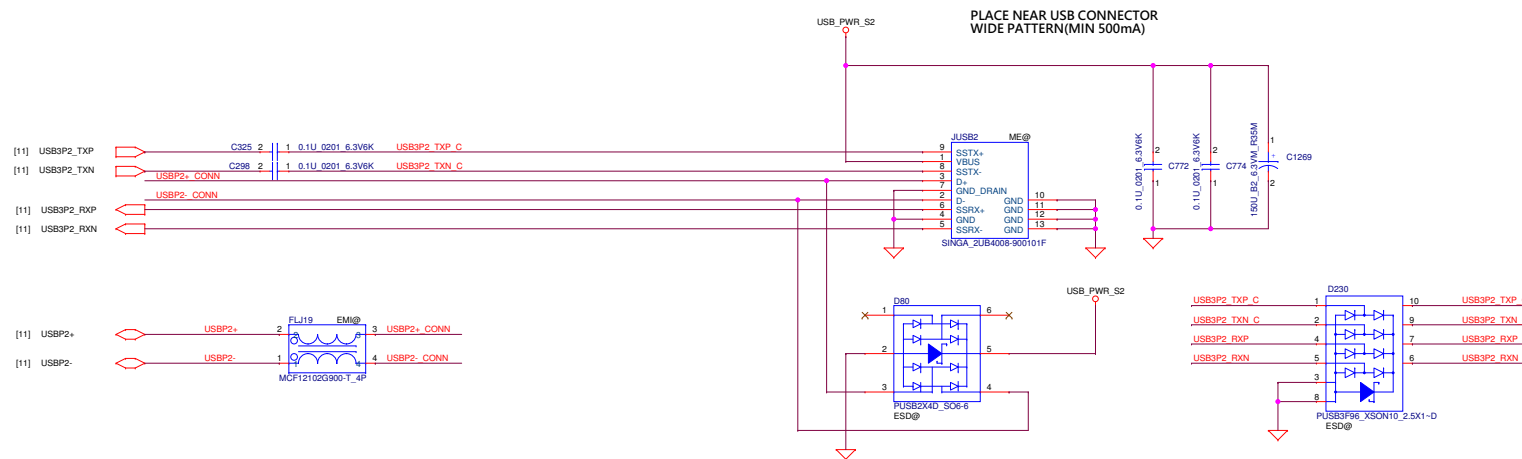


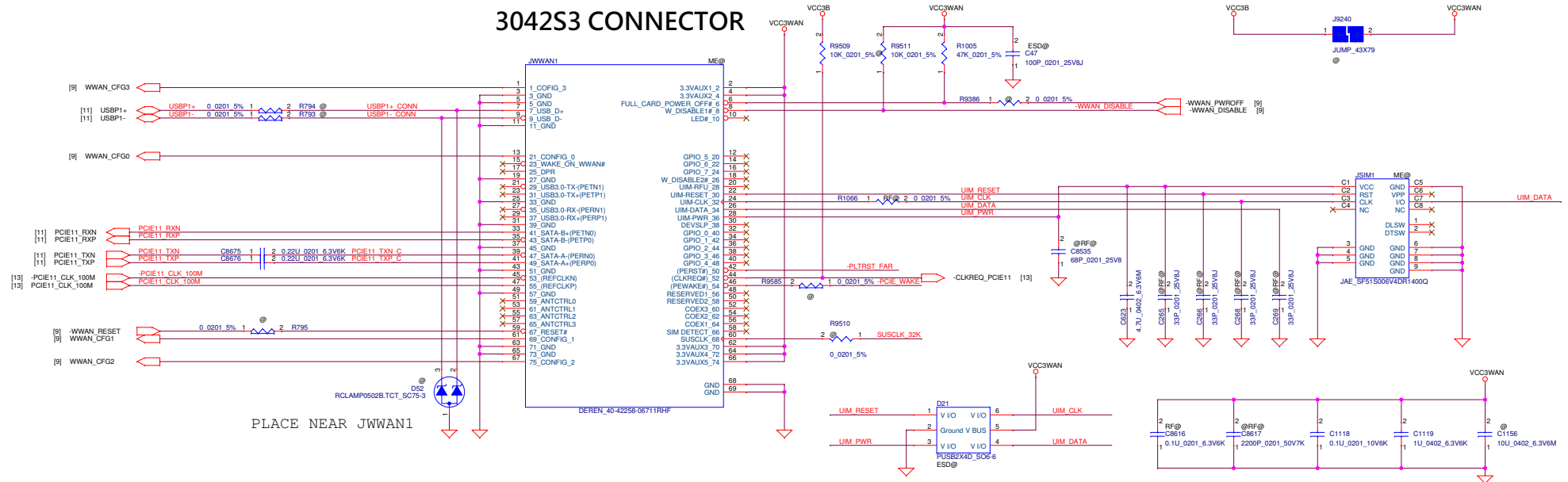
TABLE of USB3.0 Single	
TI	TPS2069CDGN-2
GMT	G548A1F51U

Change to TPS2069D (SA00002Y200)

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			Date: Monday, October 31, 2017	Sheet: 31 of 73

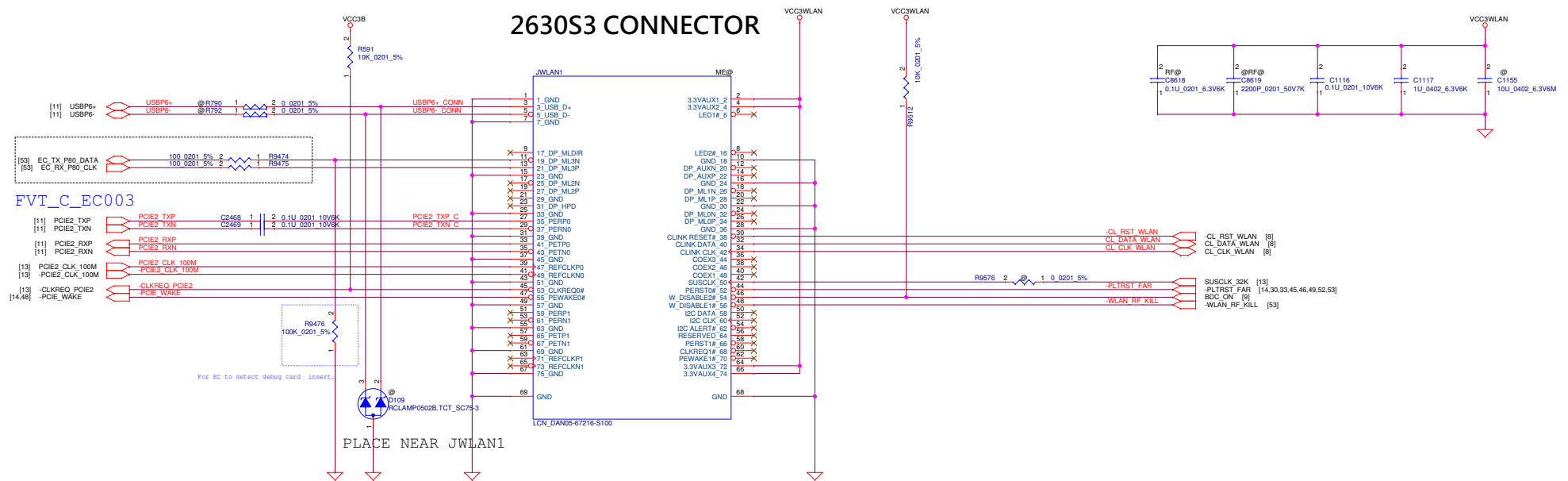
TYPE-B M.2 CARD FOR WWAN

3042S3 CONNECTOR



TYPE-A M.2 CARD FOR WLAN / Bluetooth

2630S3 CONNECTOR



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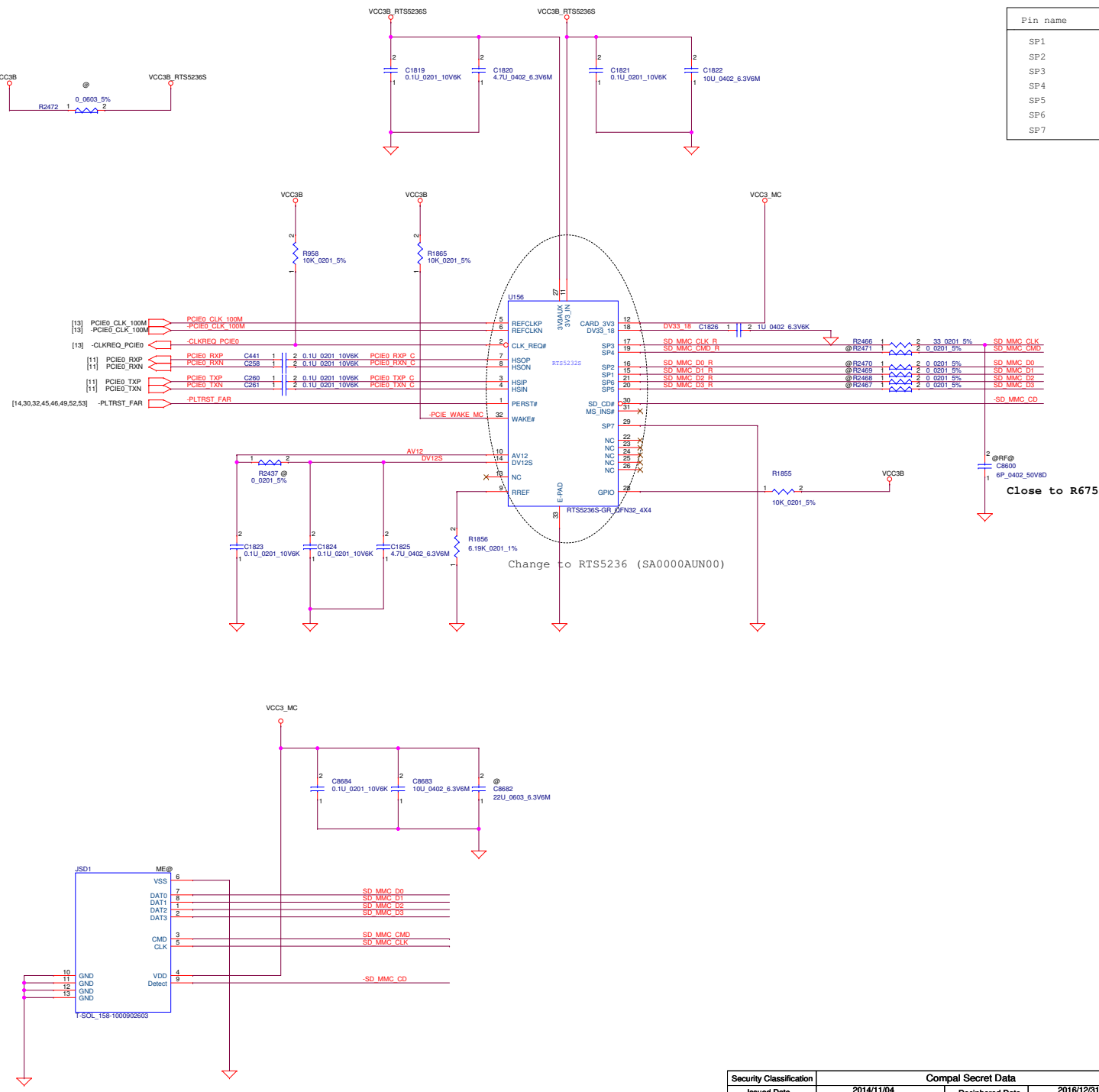
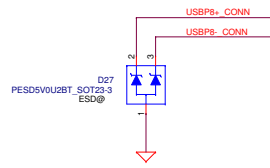
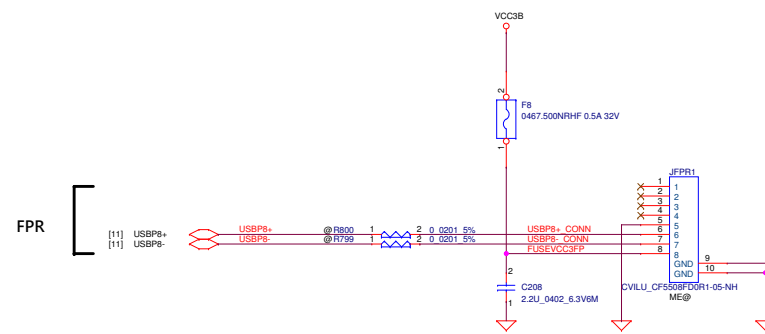
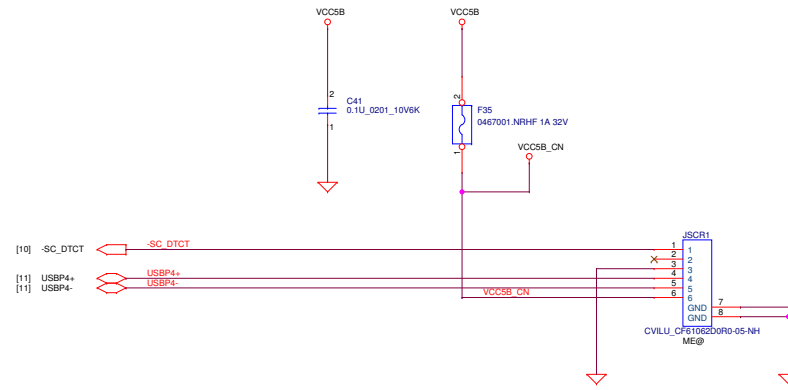


TABLE		
Pin name	SD/MMC	MEMORSTICK
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7		

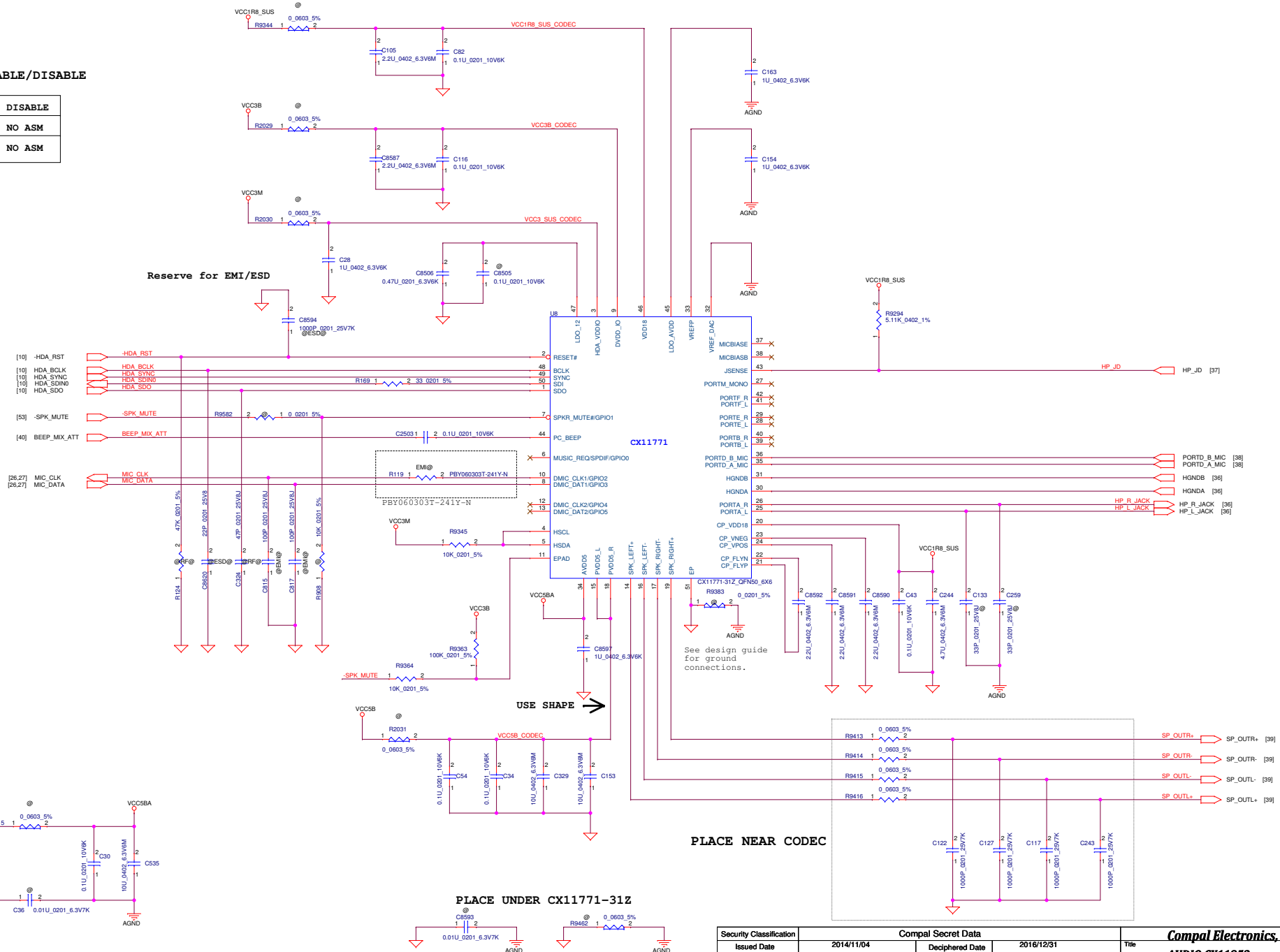


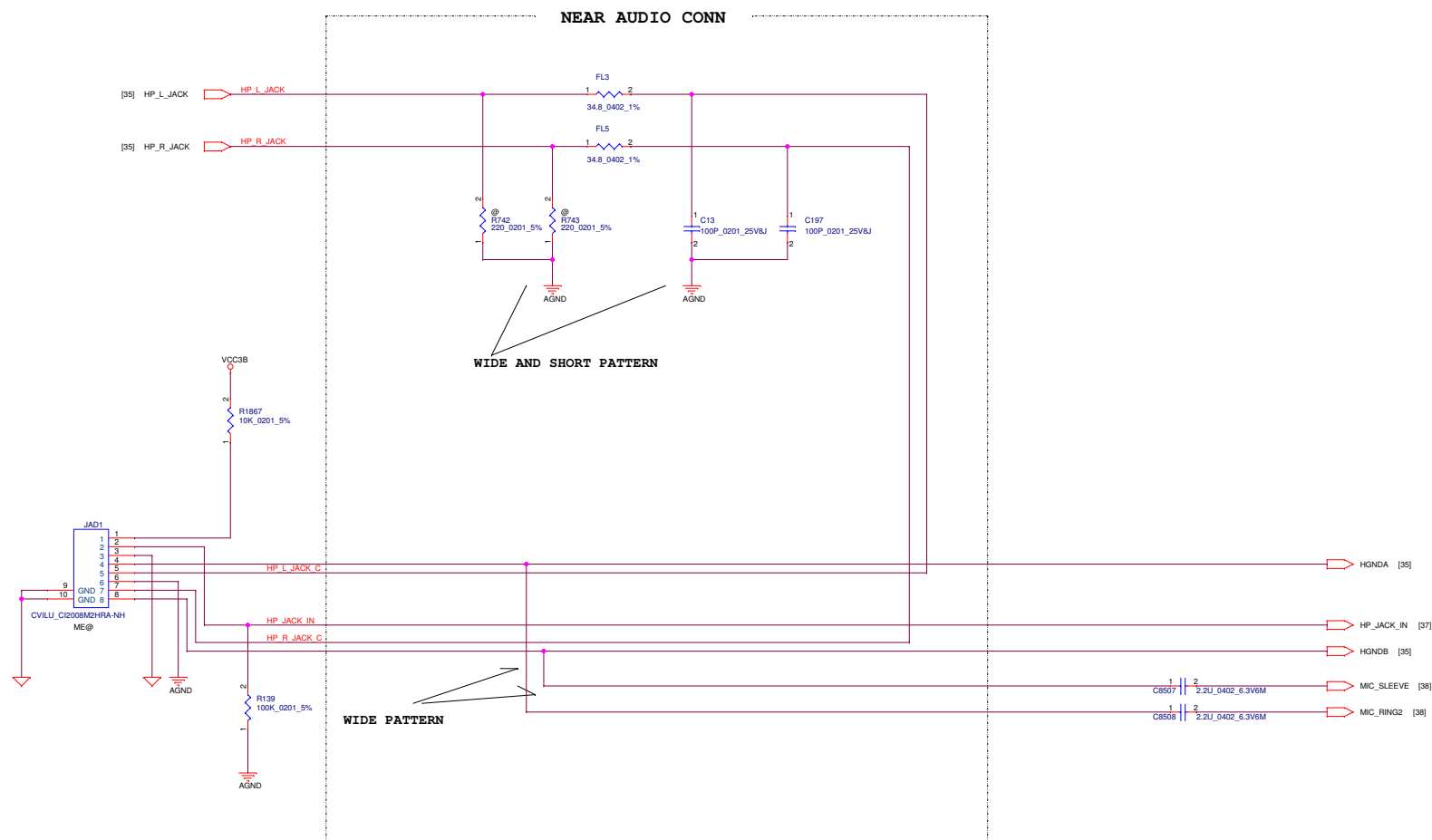
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	SMART CARD/FPR
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TABLE MIC HW ENABLE/DISABLE

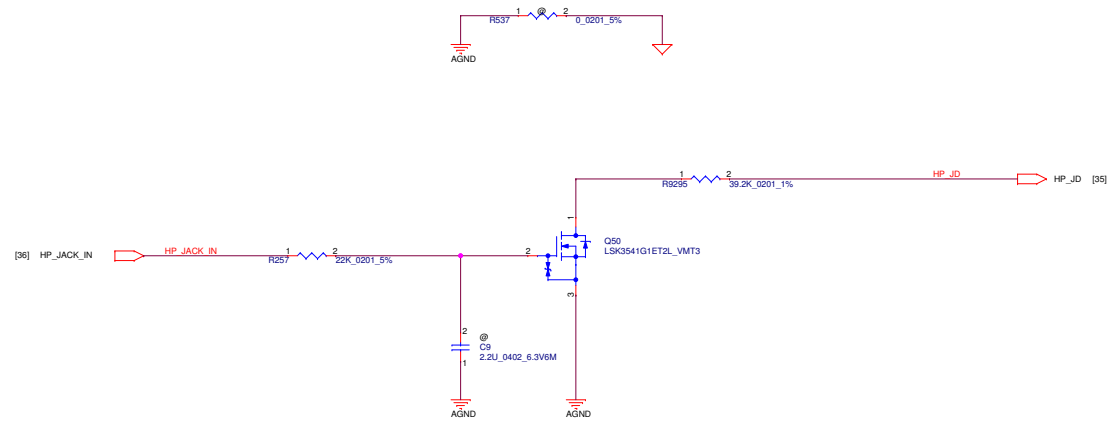
	ENABLE	DISABLE
R961	ASM	NO ASM
R119	ASM	NO ASM

LOGIC
↑

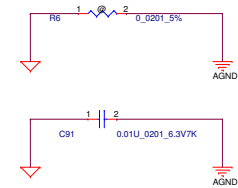
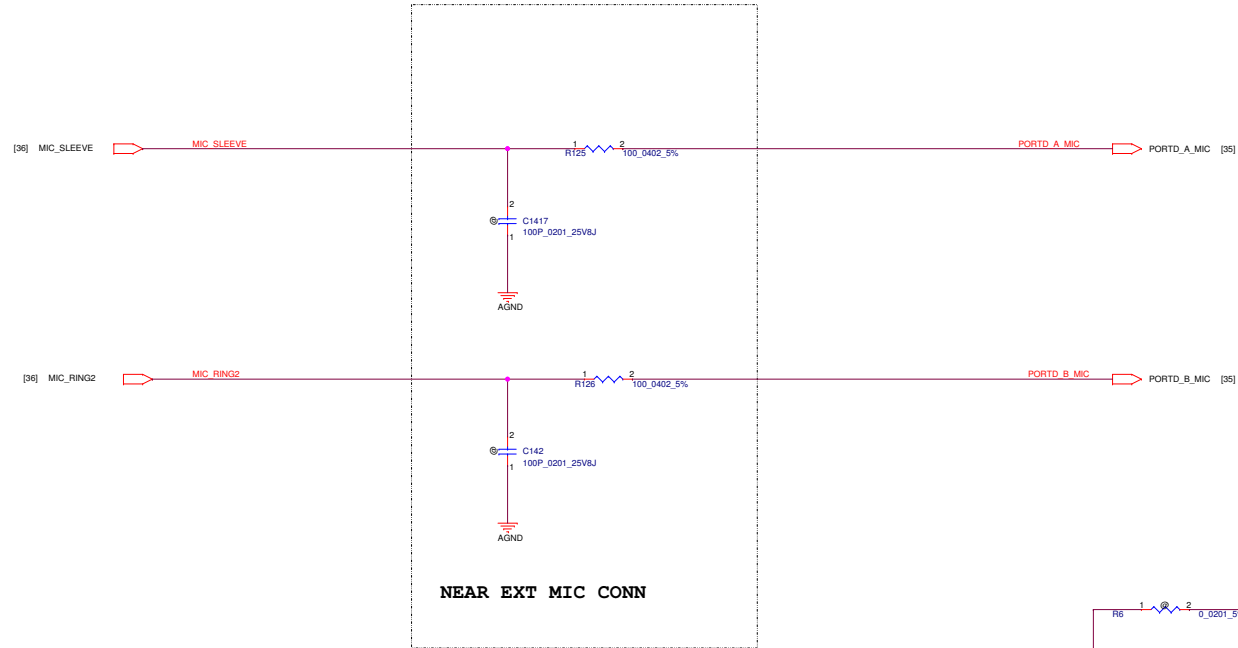




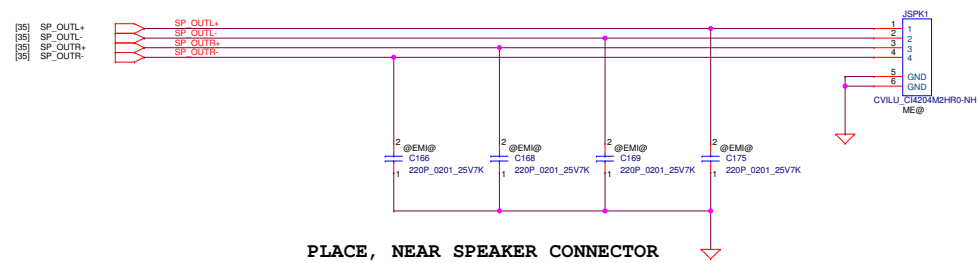
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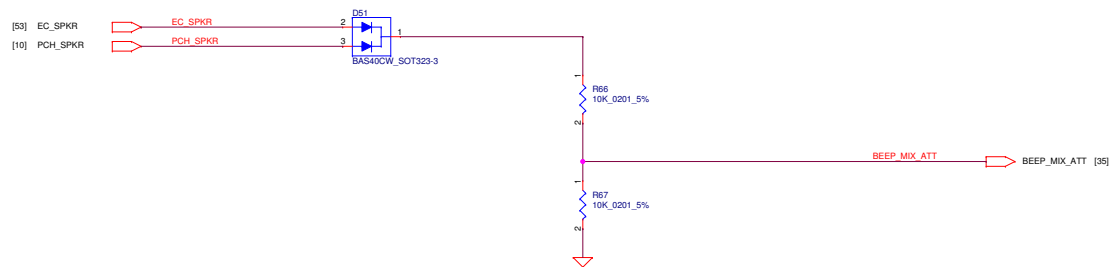
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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				LA-F421P	1.0
				Date	Monday, October 23, 2017
				Sheet	49 of 73

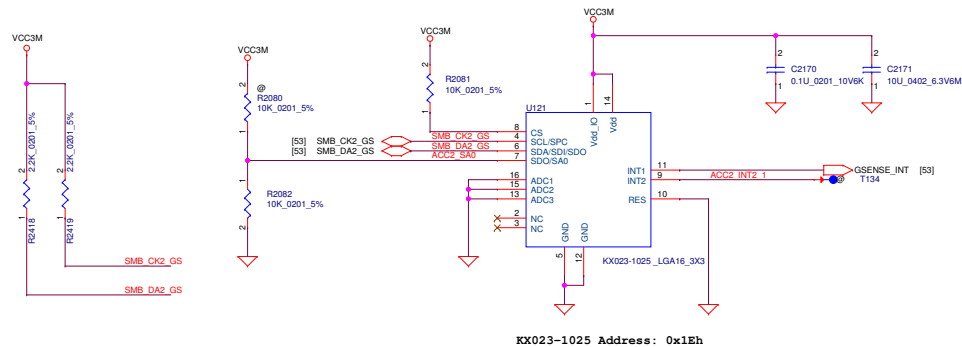
Intelligent Cooling G-Sensor

TABLE

ACC2_SA0	Address Selection
H	32h (W) & 33h (R)
L	30h (W) & 31h (R)

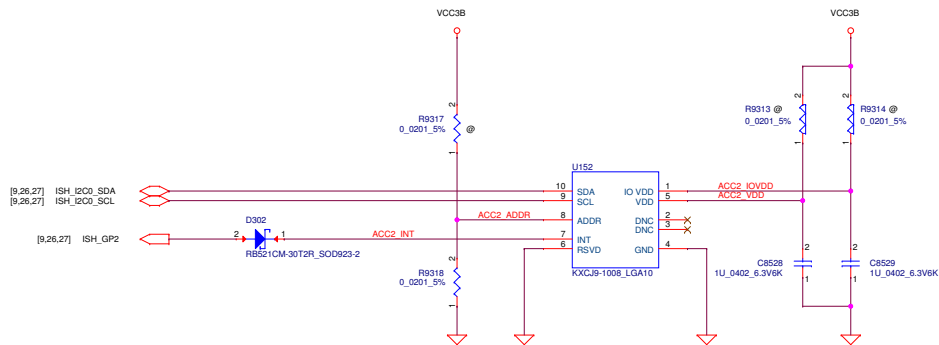
TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode



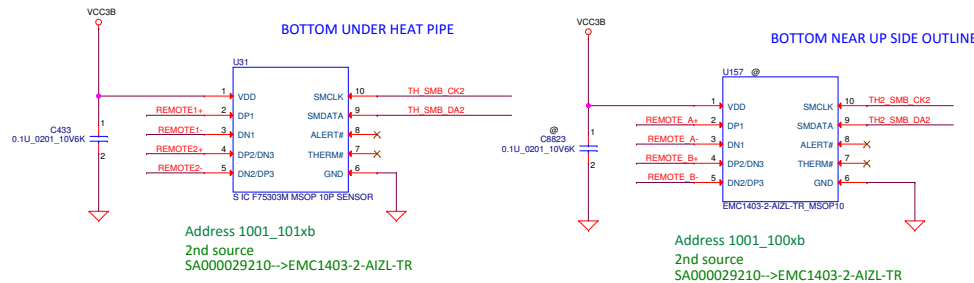
KX023-1025 Address: 0x1Eh

G-Sensor



KXCJ9 Address: 0x1Ch

Thermal Sensor

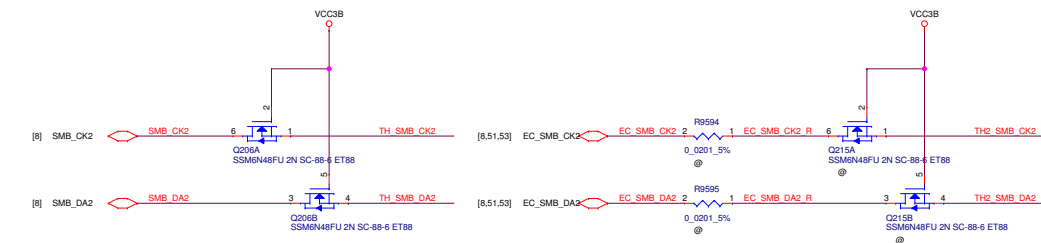
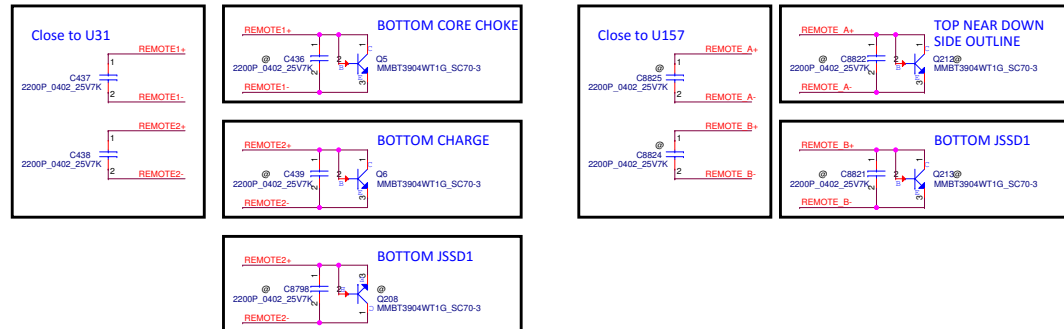


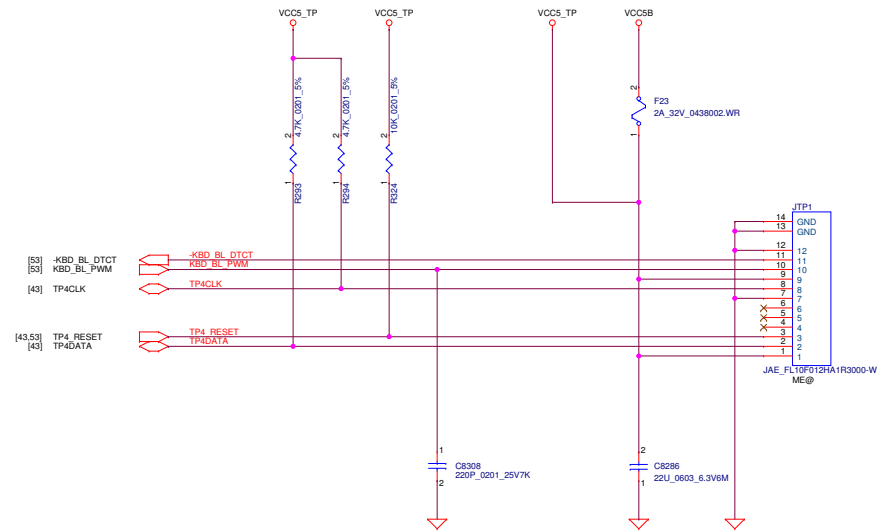
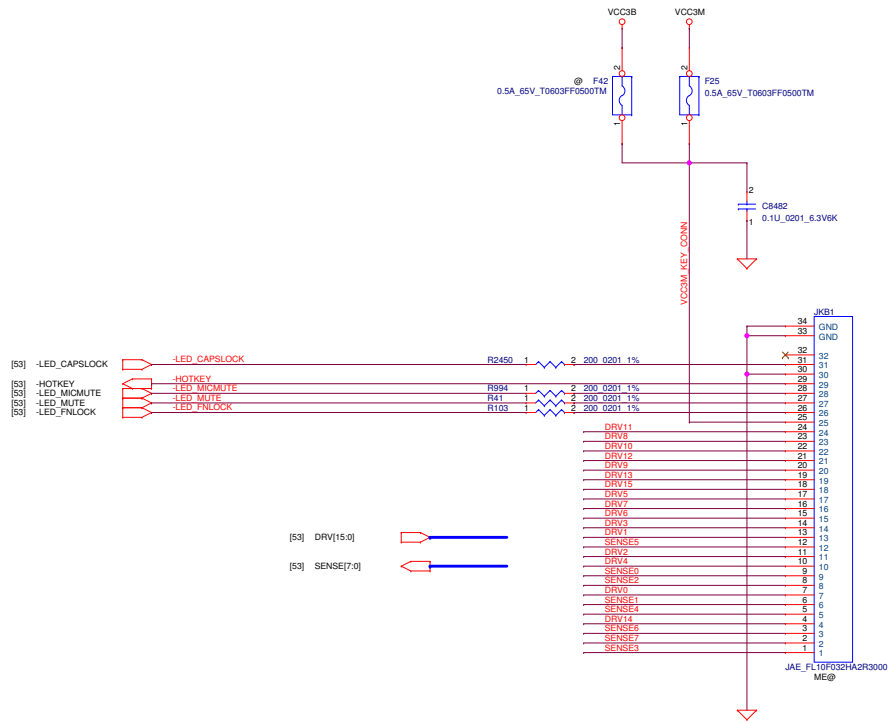
Address 1001_101xb
2nd source
SA000029210-->EMC1403-2-AIZL-TR

Address 1001_100xb
2nd source
SA000029210-->EMC1403-2-AIZL-TR

REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

REMOTEA,B (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

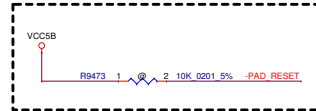
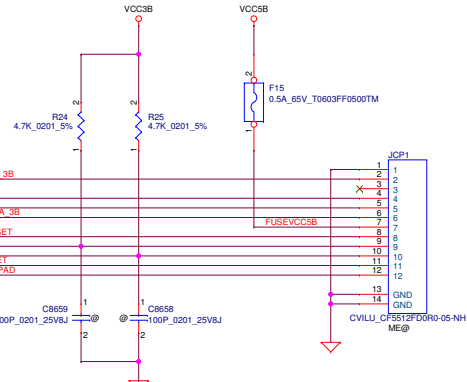




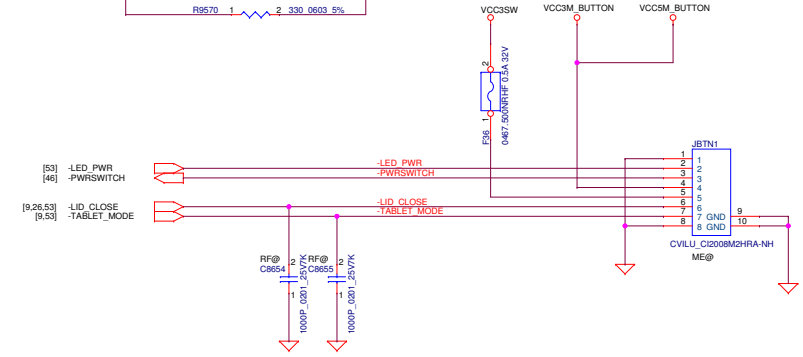
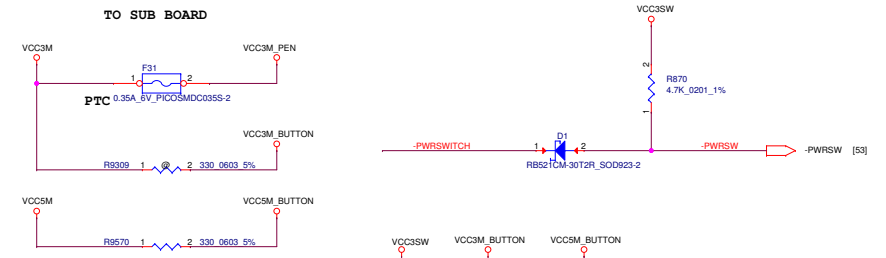
Clickpad

- [46] SMB_CLK_3B
- [42] TP4DATA
- [42] TP4CLK
- [46] SMB_DATA_3B
- [53] -PAD_RESET
- [53] IPDCLK
- [53] IPDDATA
- [42,53] TP4_RESET
- [53] BYPASS_PAD

- SMB_CLK_3B
- TP4DATA
- TP4CLK
- SMB_DATA_3B
- PAD_RESET
- IPDCLK
- IPDDATA
- TP4_RESET
- BYPASS_PAD

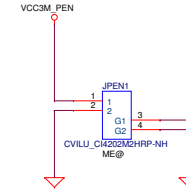
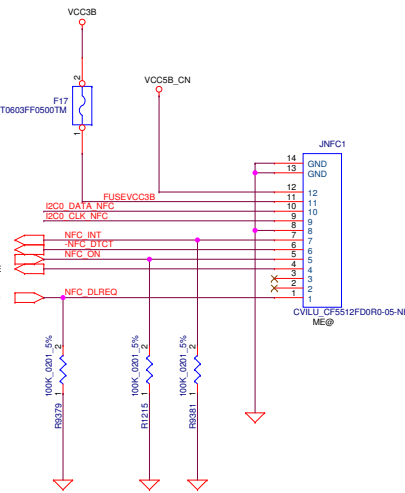


TO SUB BOARD



NFC

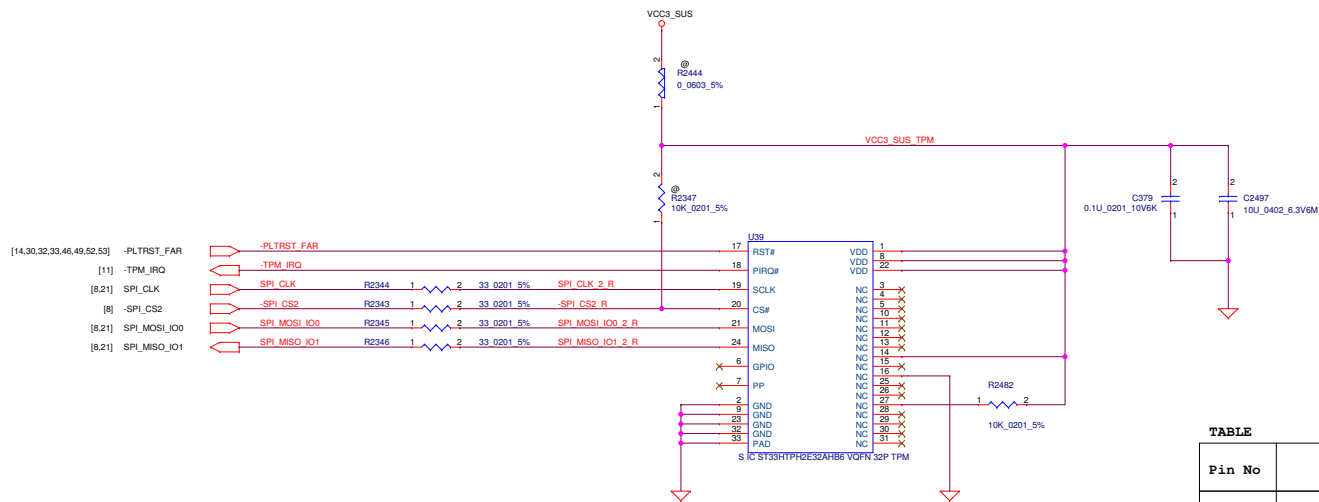
- [11] NFC_INT
- [9] NFC_DTCT
- [11] NFC_ON
- [10] NFC_ACTIVE
- [9] NFC_DLREQ



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			Date:	Monday, October 23, 2017	Sheet 44 of 73



-Change TPM1.2 to TPM2.0
-Infineon SLB9670VQ2.0 part number SA00009N230
-ST ST33HTPH2E32AHB6 part number SA00009SO40

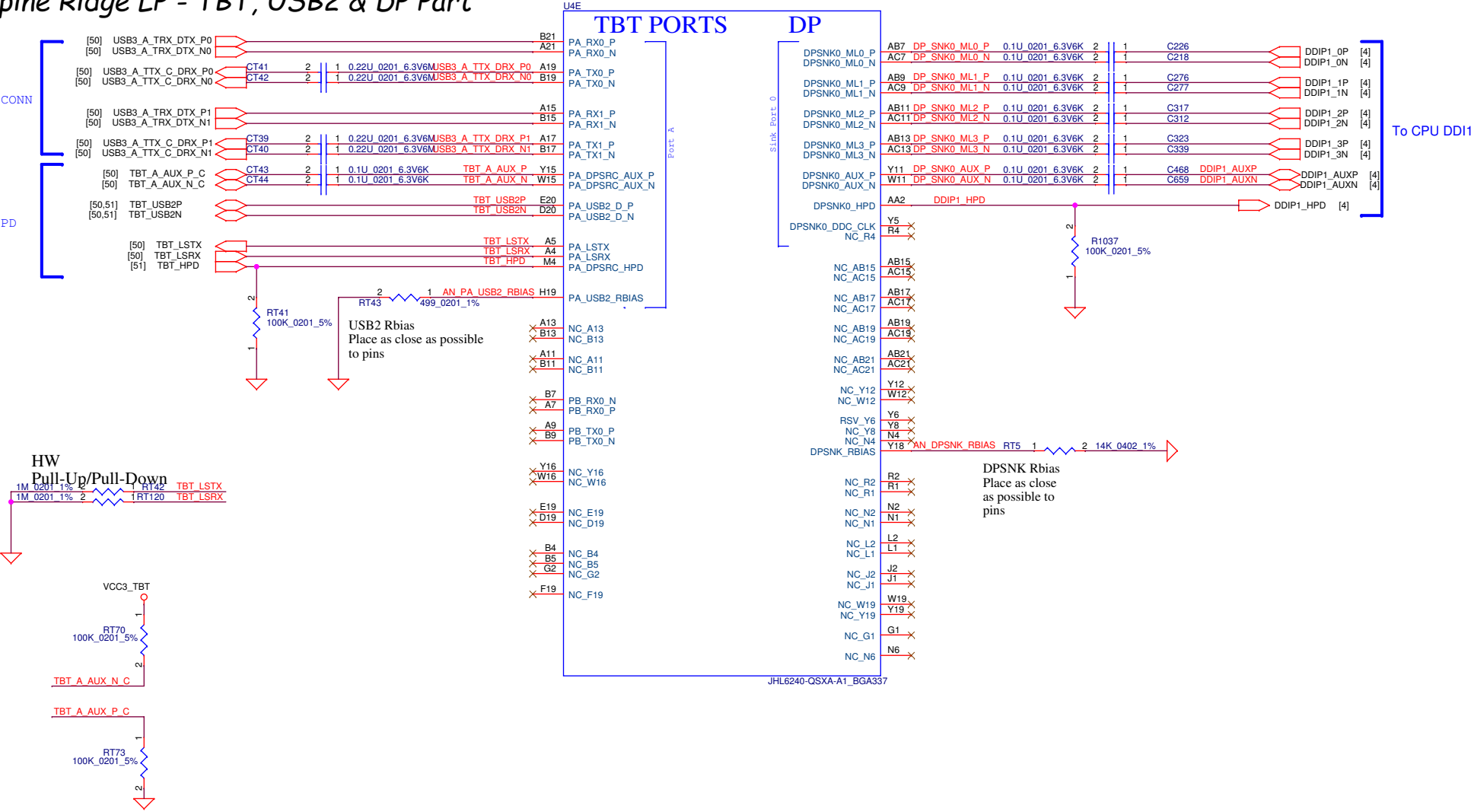
FVT_C_EC001

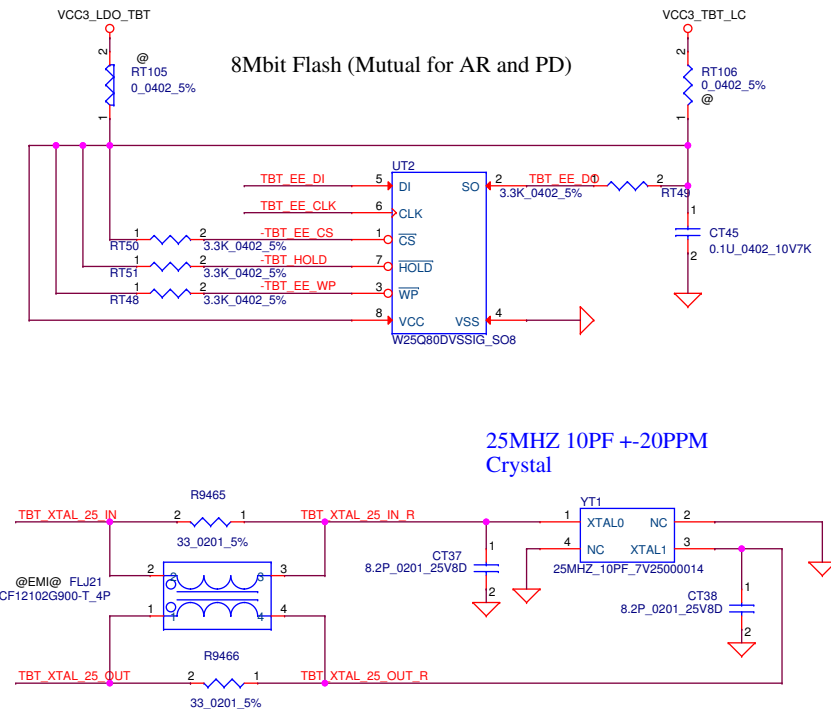
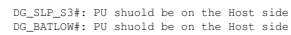
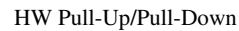
TABLE

Pin No	ST ST33HTPH2E32AHB6	Infineon SLB9670VQ2.0 FW7.61
1	NC	VDD
2	GND	GND
3	NC	NC
4	NC	NC
5	NC	NC
6	NC	GPIO
7	PP	PP
8	NC	VDD
9	NC	GND
10	NC	NC
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	VDD
15	NC	NC
16	NC	GND
17	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK
20	SPI_CS#	CS#
21	MOSI	MOSI
22	VDD	VDD
23	NC	GND
24	MISO	MISO
25	NC	NC
26	NC	NC
27	NC	NC
28	NC	NC
29	NC	NC
30	NC	NC
31	NC	NC
32	NC	GND

Alpine Ridge LP - TBT, USB2 & DP Part

Alpine Ridge LP - TBT, USB2 & DP Part

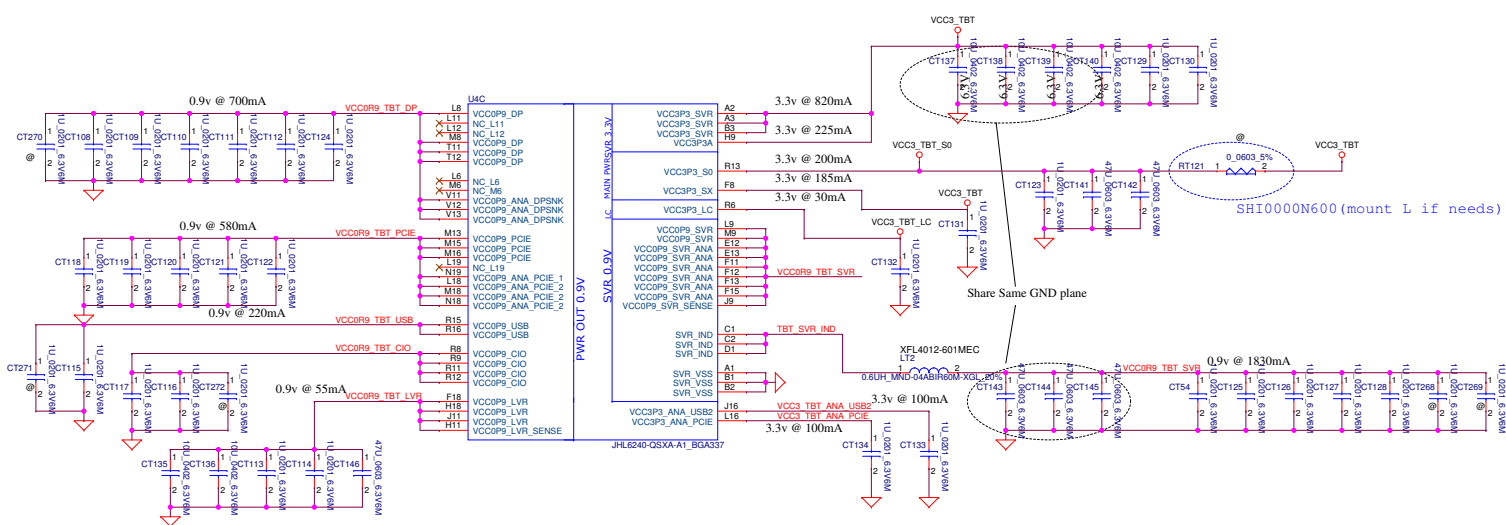


Alpine Ridge LP - Misc
Symbol

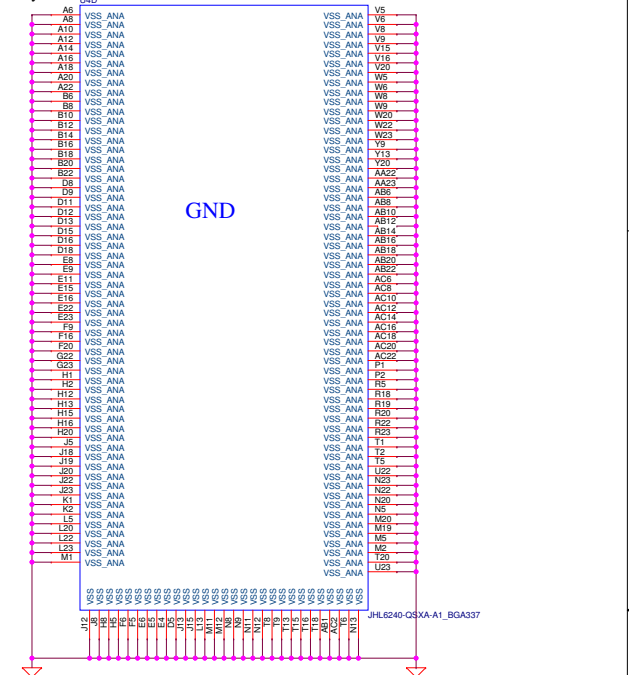
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Issued Date	2014/11/04	Deciphered Date	2016/12/31	Title	AR : MISC	
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Alpine Ridge LP - Power Supply

Alpine Ridge SP - VCC
Symbol



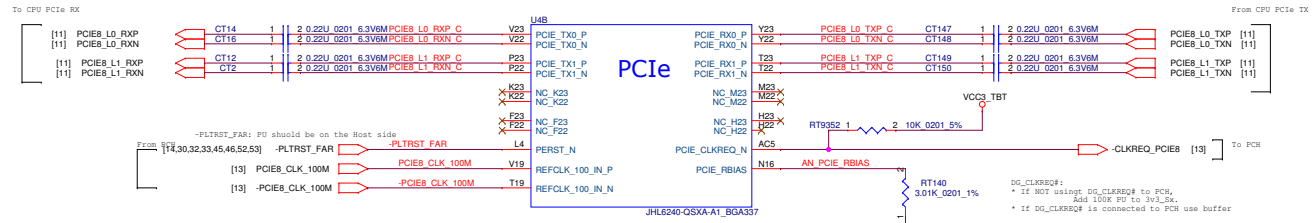
Alpine Ridge SP - GND
Symbol



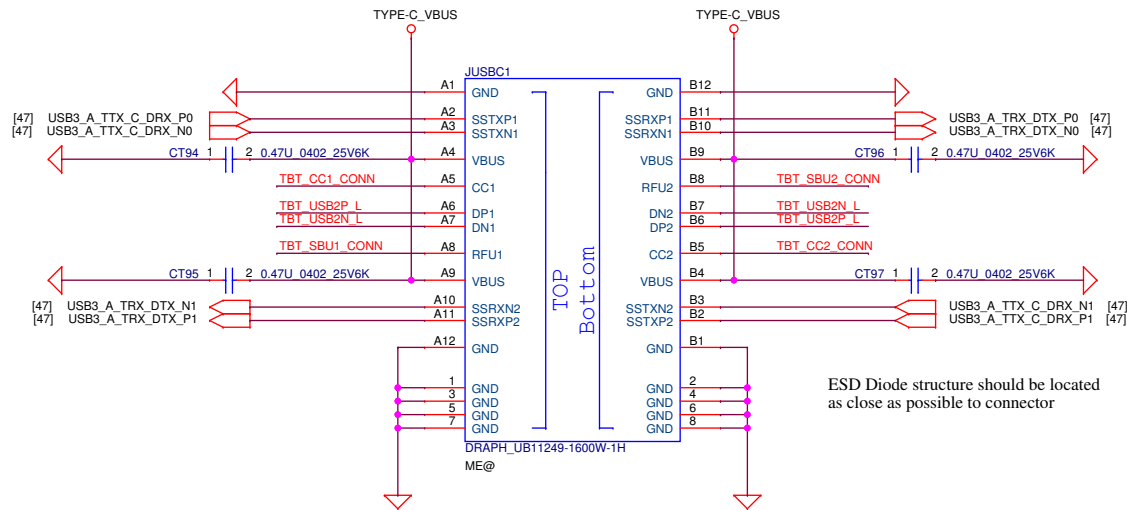
AR-LP Power & GND

AR-LP PCIE

Alpine Ridge LP - PCIE
Symbol

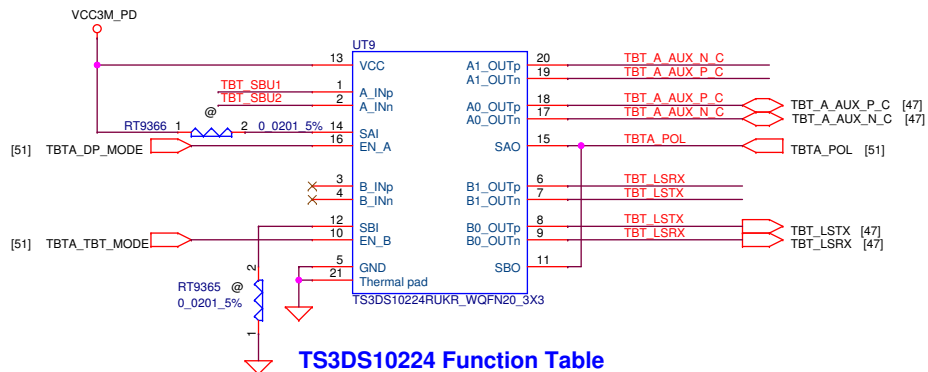
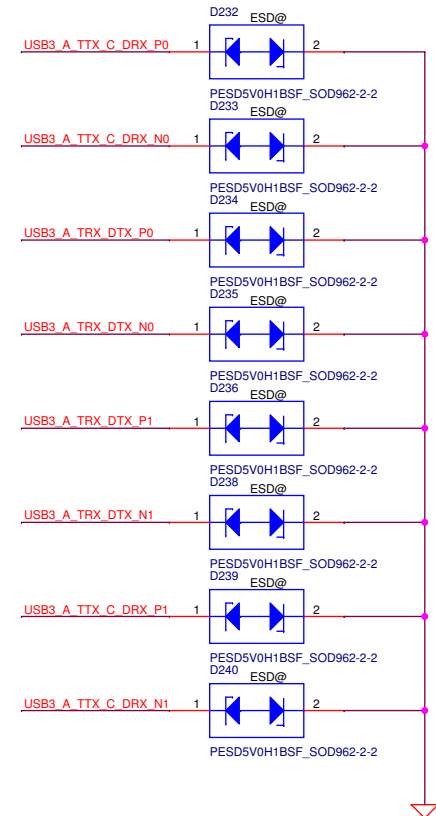
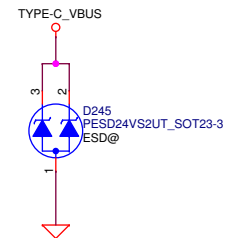
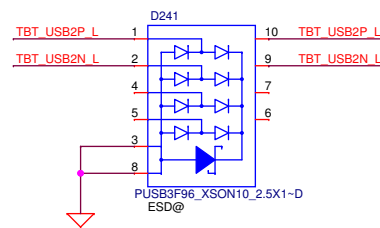


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ESD Diode structure should be located as close as possible to connector

ESD for USB2 Lines and Control lines

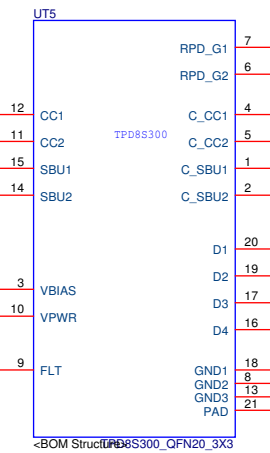
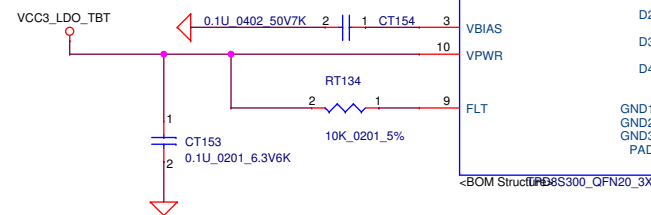
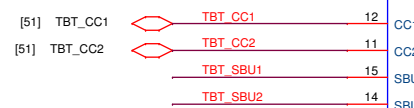
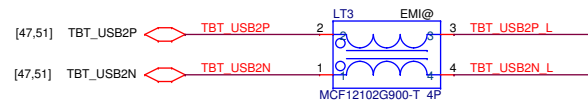


TS3DS10224 Function Table

SBU1	SBU2	(ENA) PA DP Mode	(ENB) PA TBT Mode	(SAO/SBO) PA POL	OUTA0	OUTA1	OUTB0	OUTB1
Hi-Z	Hi-Z	0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
AUX_P	AUX_N	1	0	0	INA	Hi-Z	Hi-Z	Hi-Z
AUX_N	AUX_P	1	0	1	Hi-Z	INA	Hi-Z	Hi-Z
LSTX	LSRX	0	1	0	Hi-Z	Hi-Z	INA	Hi-Z
LSRX	LSTX	0	1	1	Hi-Z	Hi-Z	INA	INA

ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z	EN	EN
1	0	EN	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN	EN

SAI/SAO/SBI/SBO	OUTA0	OUTA1	OUTB0	OUTB1
1 0 0 0	INA	Hi-Z	INA	Hi-Z
1 1 0 1	Hi-Z	INA	Hi-Z	INA

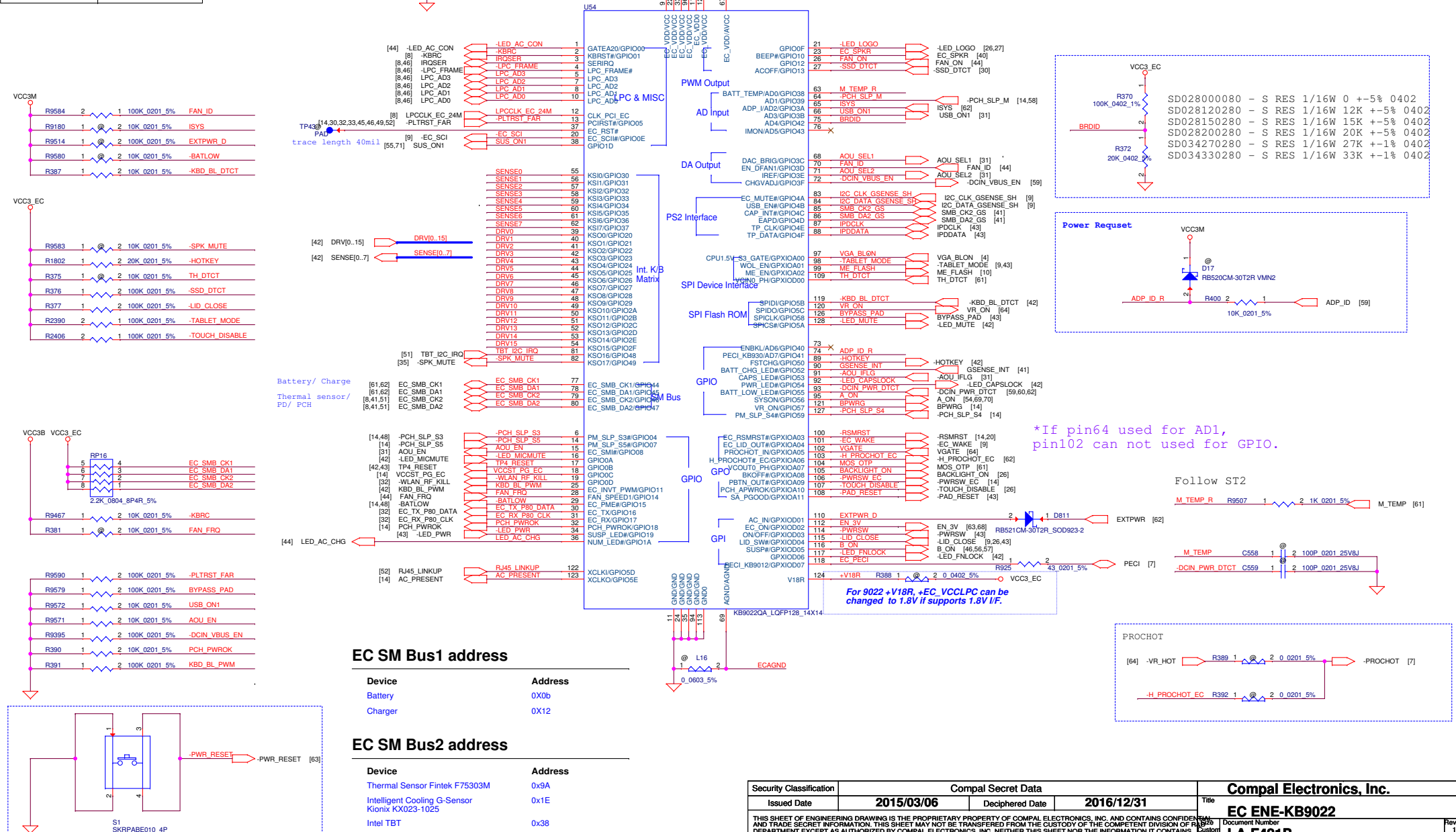


EC KB9022

KB9022 A v.02

GPIO W/O internal-PH:

- | | |
|-----------|------------|
| 1. GPIO44 | 6. GPIO4B |
| 2. GPIO45 | 7. GPIO4E |
| 3. GPIO46 | 8. GPIO4F |
| 4. GPIO47 | 9. GPIO50 |
| 5. GPIO4A | 10. GPIO51 |

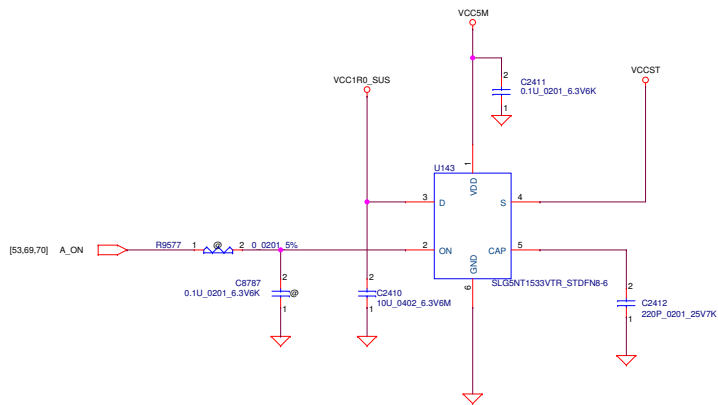


Vcc	3.3V +/- 5%				
R370	100K +/- 1%				
Board ID	R372	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD
SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
FVT	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
SIT	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
SVT	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
TBD	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
TBD	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
TBD	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54

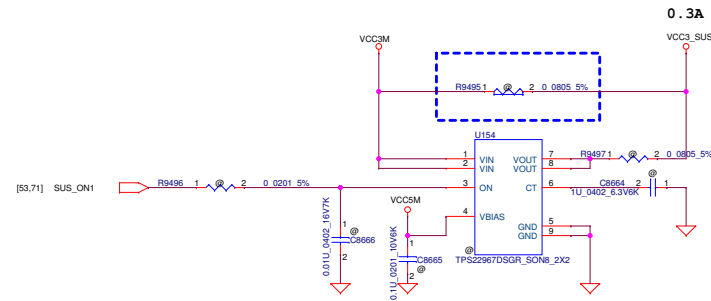
EC SM Bus1 addressEC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	0x9A
Intelligent Cooling G-Sensor Kionix KX023-1025	0x1E
Intel TBT	0x38

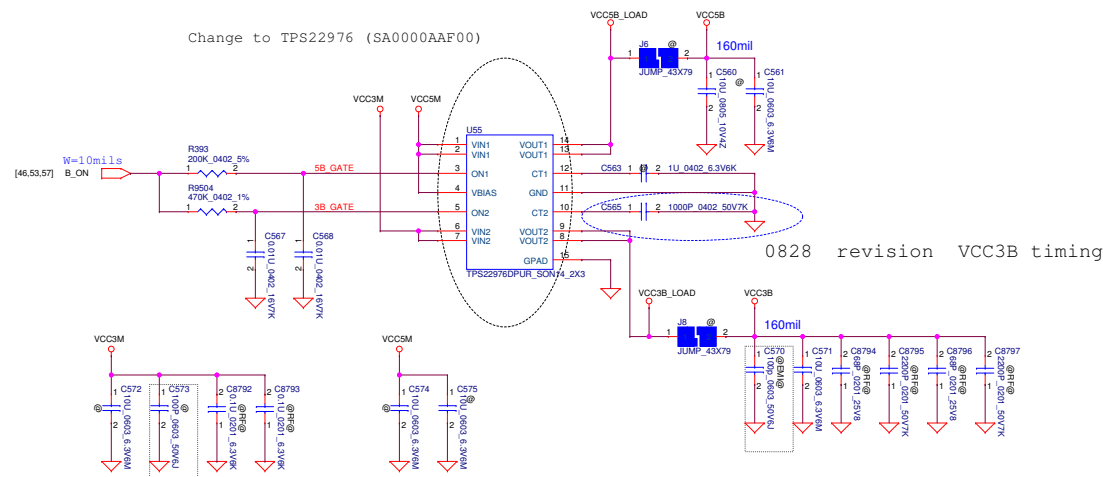
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				Customer	LA-F421P	
Date: Monday, October 23, 2017				Sheet	53	of 73



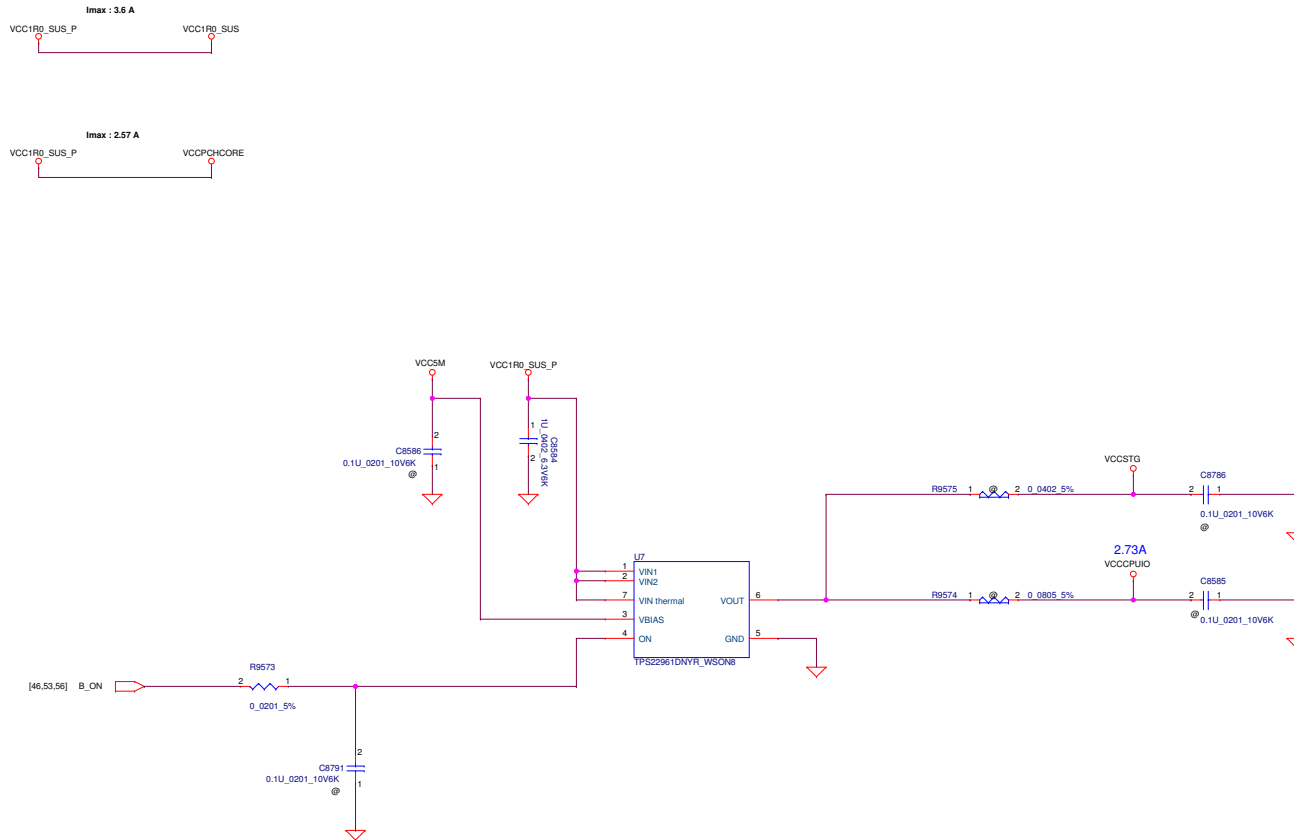
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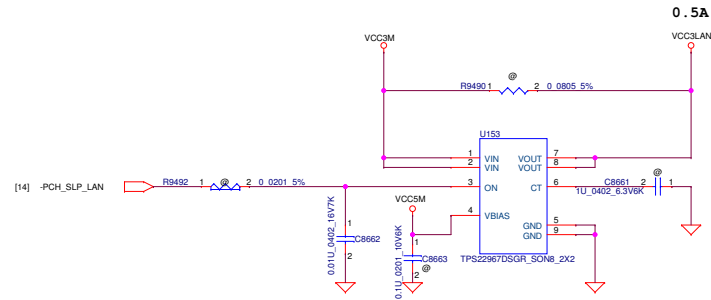
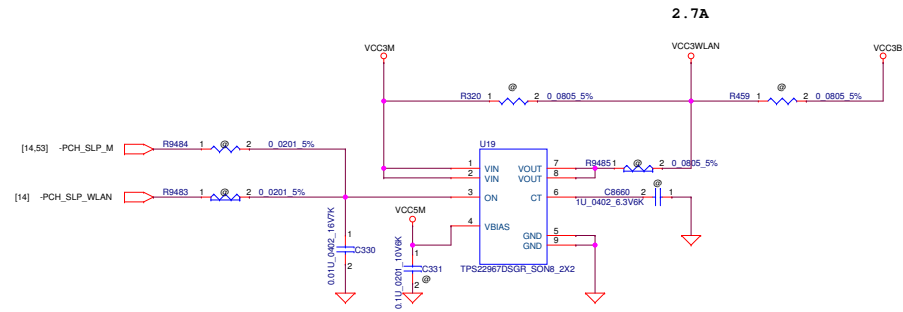
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2014/11/04		2016/12/31		Title	
2016/12/31		2016/12/31		LOAD SW PCH SUS/TRACK POIN	
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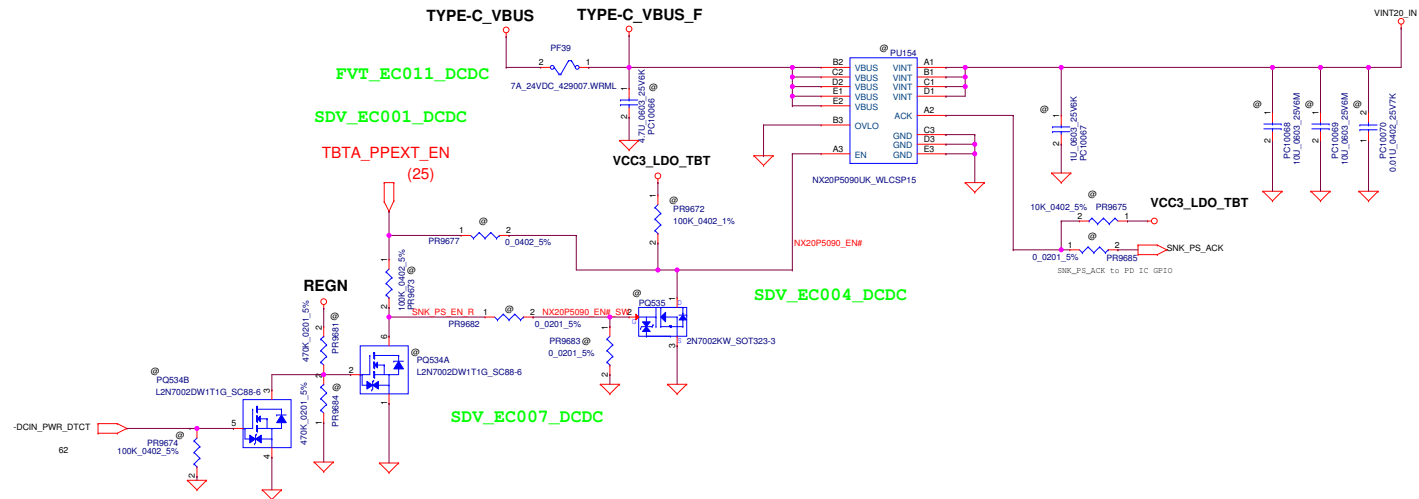
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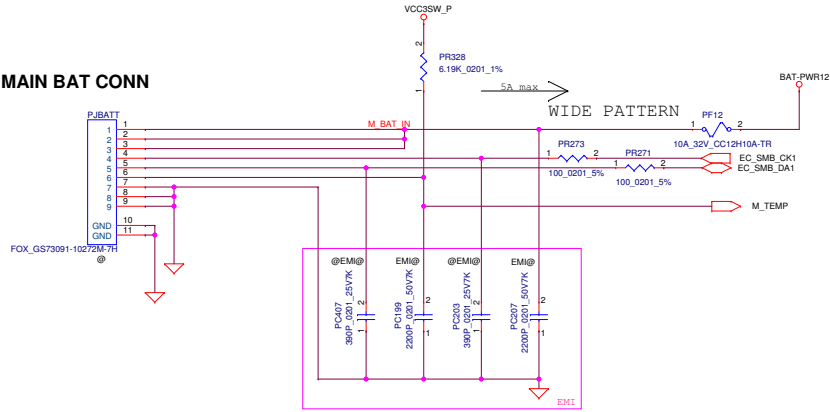


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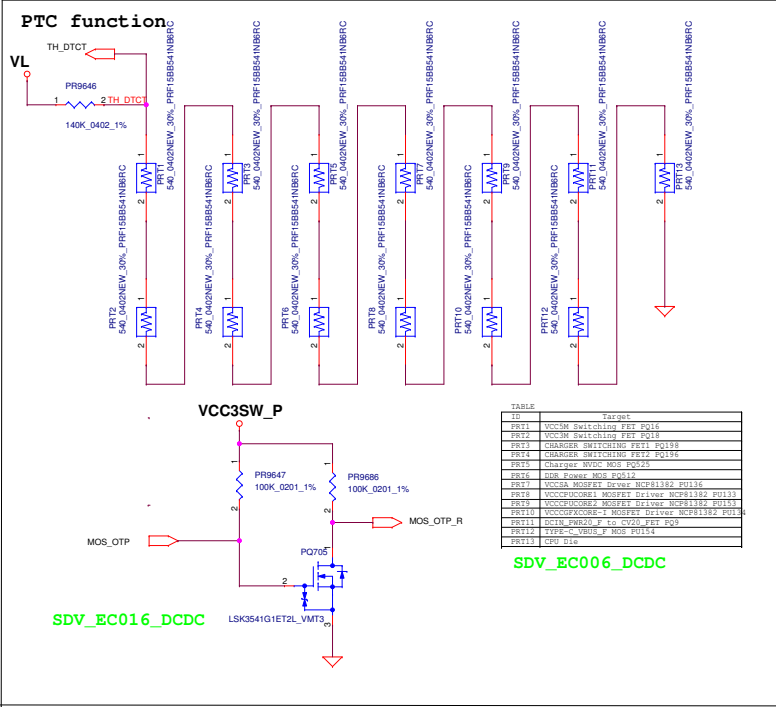


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MAIN BAT CONN



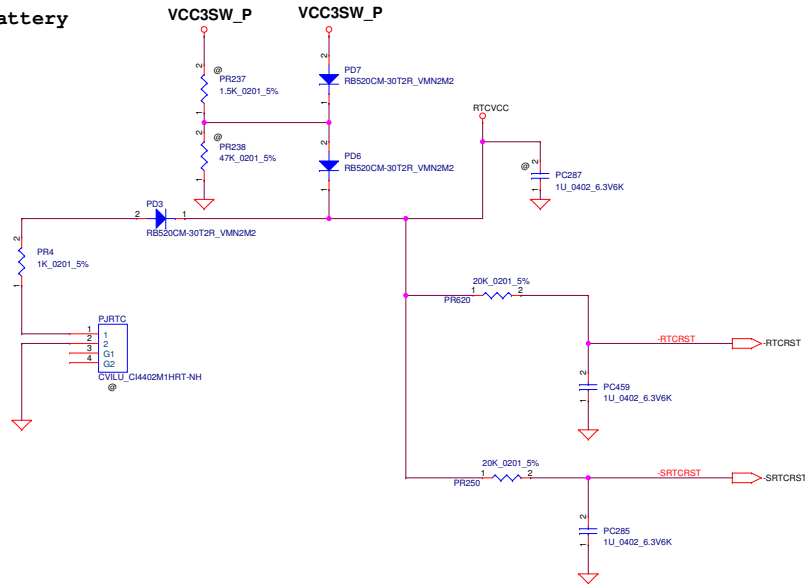
SDV_EC008_DCDC



ID	TABLE
PR21	VCC3M Switching FET P016
PR22	VCC3M Switching FET P018
PR23	CHARGER SWITCHING FET P019
PR24	CHARGER SWITCHING FET P019
PR25	CHARGER SWITCHING FET P019
PR26	CHARGER SWITCHING FET P019
PR27	VCC3M Switching FET P016
PR28	VCC3M Switching FET P018
PR29	VCC3M Switching FET P018
PR30	VCC3M Switching FET P018
PR31	VCC3M Switching FET P018
PR32	VCC3M Switching FET P018
PR33	VCC3M Switching FET P018

SDV_EC006_DCDC

RTC Battery

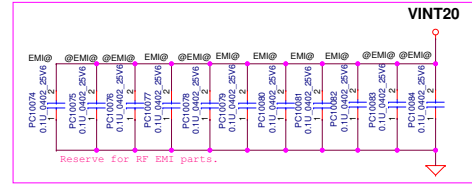


Should be placed near ACP, ACN

Keep these two signals as a pair routing

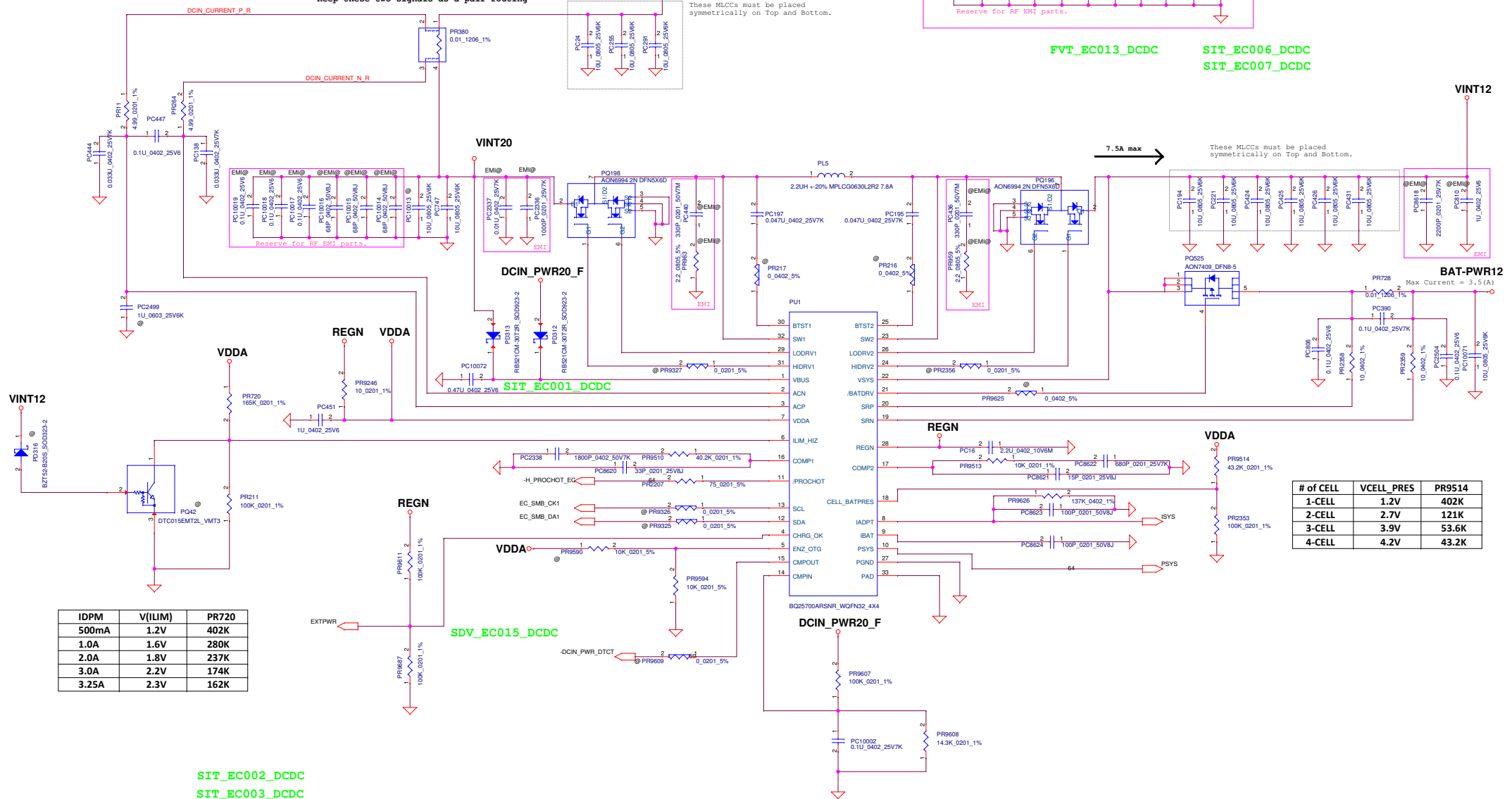
VINT20_IN
Max Current = 3.25(A)

These MLCCs must be placed symmetrically on Top and Bottom.



FVT_EC013_DCDC

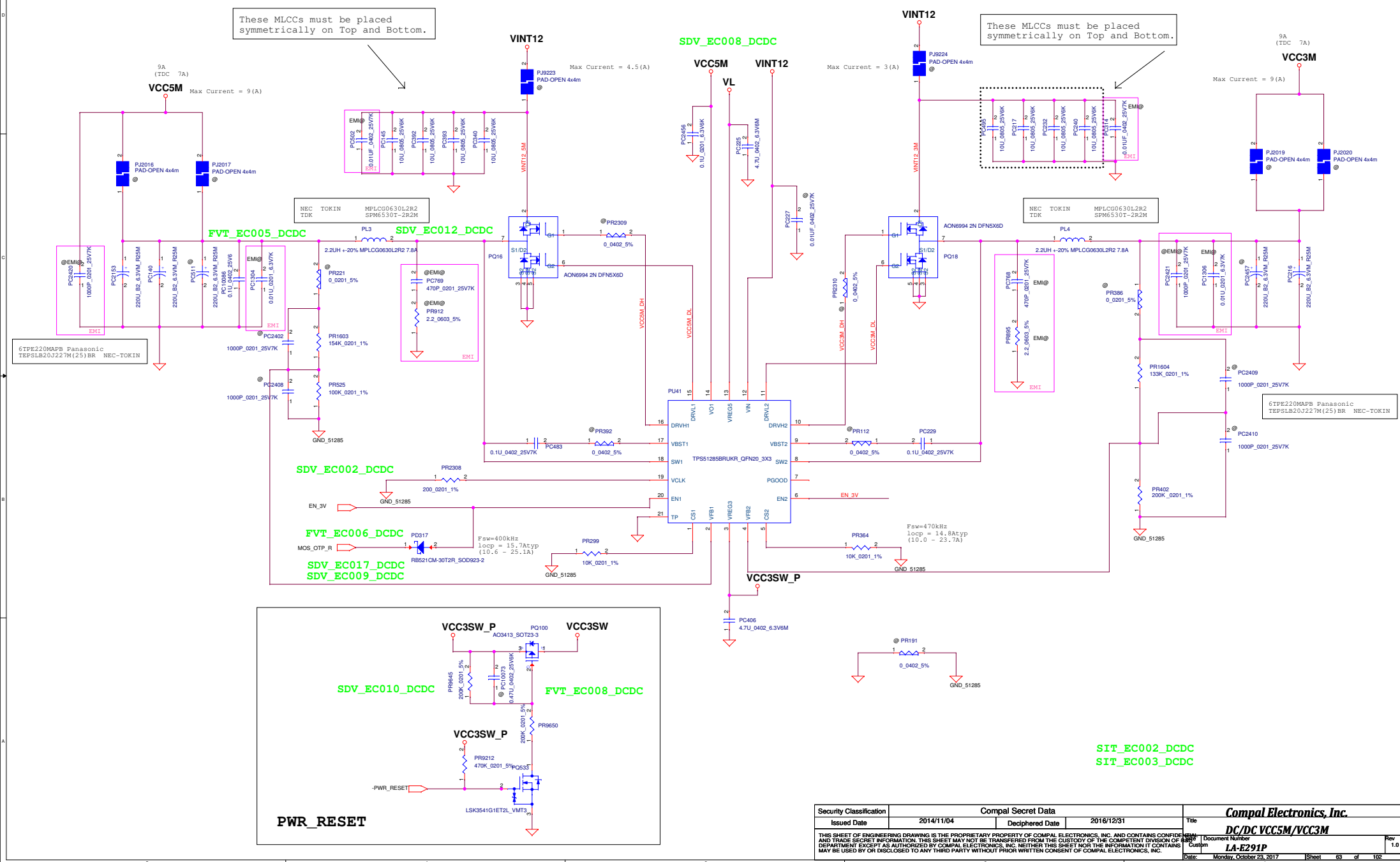
SIT_EC006_DCDC
SIT_EC007_DCDC



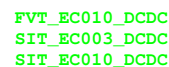
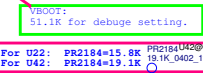
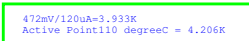
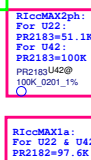
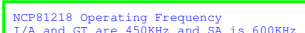
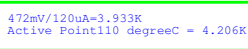
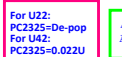
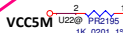
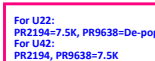
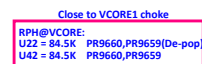
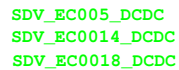
IDPM	V(ILIM)	PR720
500mA	1.2V	402K
1.0A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K


SIT_EC002_DCDC
SIT_EC003_DCDC

# of CELL	VCELL PRES	PR9514
1-CELL	1.2V	402K
2-CELL	2.7V	121K
3-CELL	3.9V	53.6K
4-CELL	4.2V	43.2K



KBL-R U42: PR9657 / PR9658
KBL-U 22: PR9655



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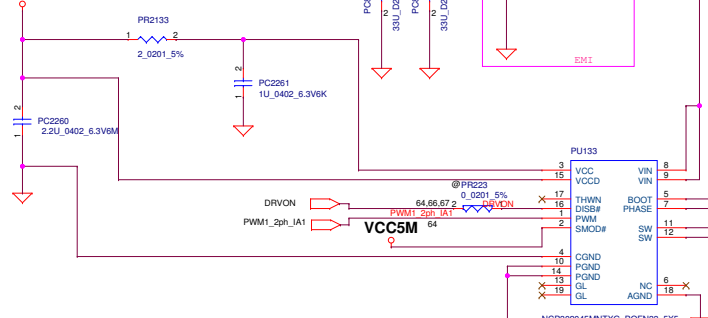
SIT_EC005_DCDC

VINT12

Max Current = 3.50(A)

These MLCCs must be placed symmetrically on Top and Bottom.

VCC5M



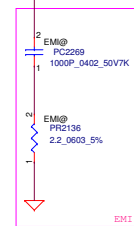
SIT_EC009_DCDC

VCCCPUCORE

TABLE PL29

CYNTEC, PCME063T-R15MS0R907

Max Current = 28(A)

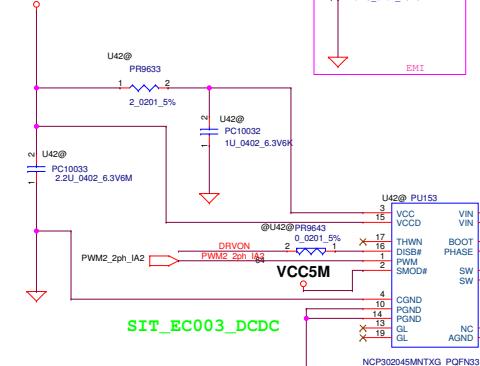


VINT12

Max Current = 3.50(A)

These MLCCs must be placed symmetrically on Top and Bottom.

VCC5M



SIT_EC003_DCDC

FVT_EC001_DCDC

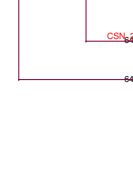
SIT_EC009_DCDC

VCCCPUCORE

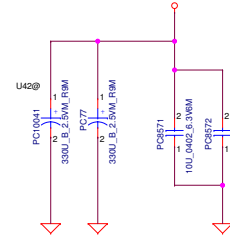
TABLE PL46

CYNTEC, PCME063T-R15MS0R907

Max Current = 28(A)

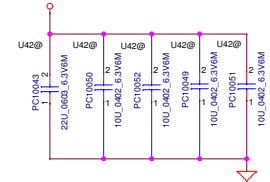


VCCCPUCORE

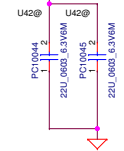


1pcs 22uF / 4pcs 10uF for VCCCPUCORE<U42>

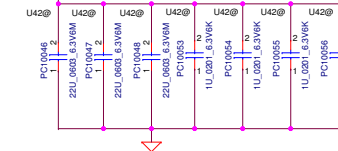
VCCCPUCORE



2pcs 22uF for VCCGFXCORE_X_VCCCPUCORE<U42>
for VCCGFXCORE_X_VCCCPUCORE

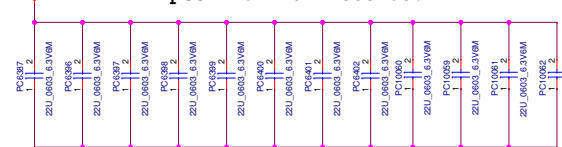


3pcs 22uF / 4pcs 1uF for VCCGFXCORE_I_VCCCPUCORE<U42>
for VCCGFXCORE_I_VCCCPUCORE



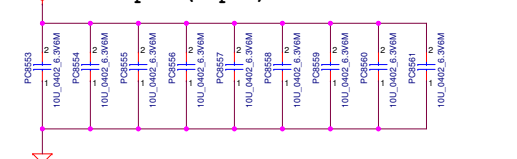
VCCCPUCORE

12pcs 22uF for VCCCPUCORE



VCCCPUCORE

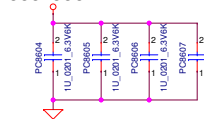
18pcs (+2pcs) 10uF for VCCCPUCORE



VCCCPUCORE

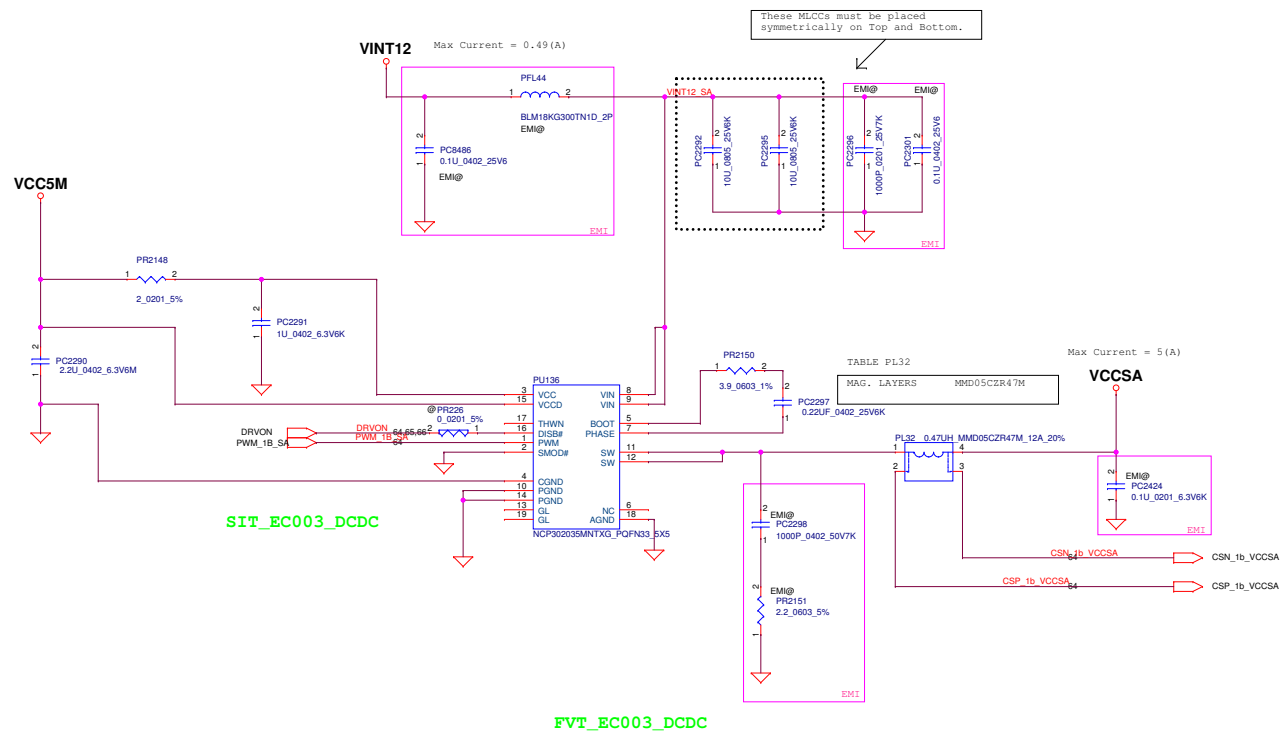
VCCCPUCORE

4pcs 1uF for VCCCPUCORE

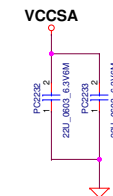
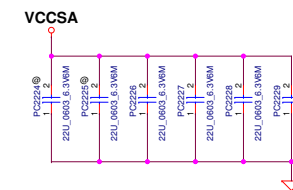


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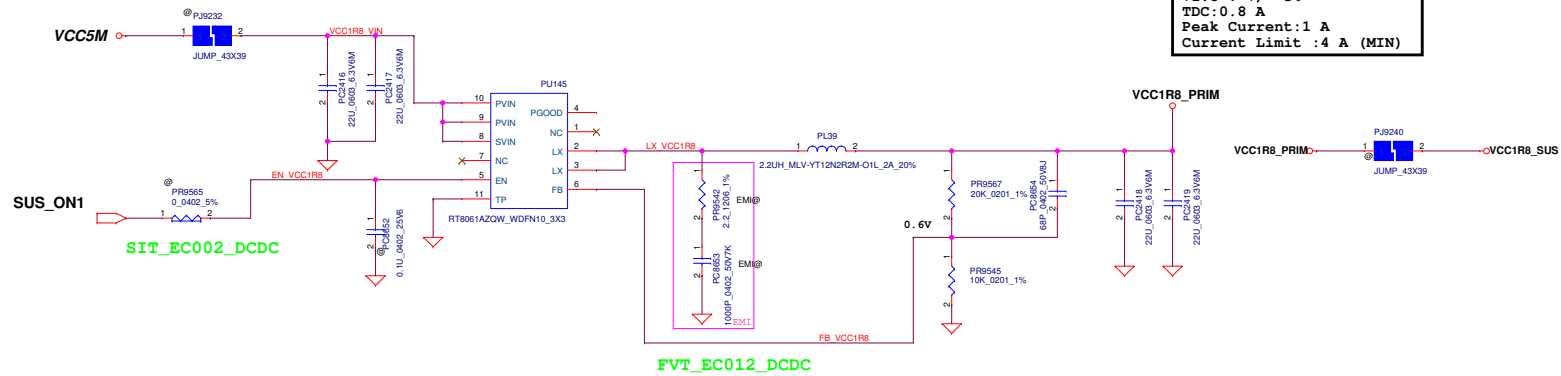
Main Func = CPUcore IA/GT/SA



6pcs (+2pcs) 22uF for VCCSA

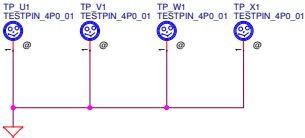
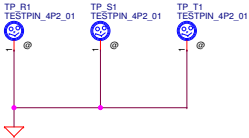
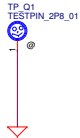
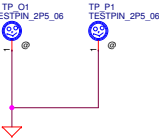
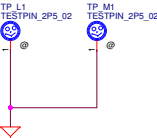
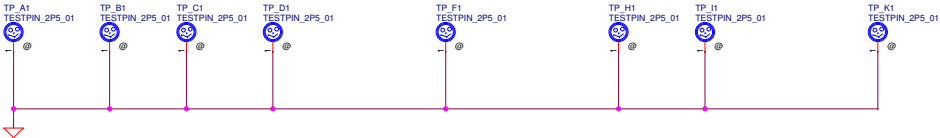


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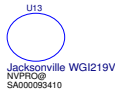
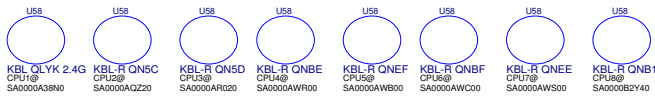
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Value	Hole Dia	Pad Dia		Qty
		TOP	BOTTOM	
TESTPIN_2P5_01	2.5	6	6	10
TESTPIN_2P5_02	2.5	7.4	7.4	2
TESTPIN_2P5_03	2.5	Square	0	1
TESTPIN_2P5_06	2.5	5	5	2
TESTPIN_2P8_01	2.8	0	Square	1
TESTPIN_4P3_01	4.3	6.5	6.5	3
TESTPIN_4P0_01	4.0	6.1	6.1	4



FID
Board Area





BOM Structure Table

BTO Item	BOM Structure	Remark
vPRO LAN chip	VPRO@	WGI219LM
non vPRO LAN chip	NVPRO@	WGI219V
Thunderbolt requirement	TBT@	
Thunderbolt reserve	@TBT@	
ESD requirement	ESD@	
ESD reserve	@ESD@	
EMI requirement	EMI@	
EMI reserve	@EMI@	
RF requirement	RF@	
RF reserve	@RF@	
XDP	XDP@	
On board RAM	X76@	
2+2 CPU	U22@	
4+2 CPU	U42@	